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POWER TRANSISTOR STABILITY AND RELIABILITY

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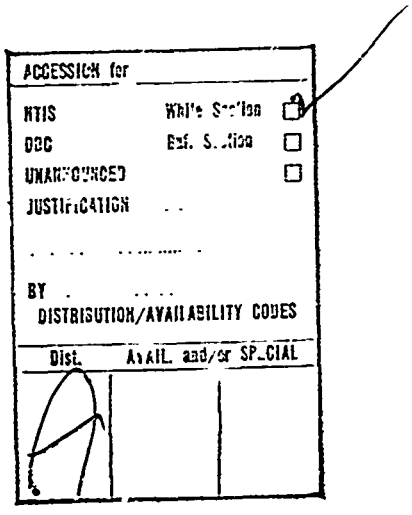

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A theoretical model has been developed for the prediction of forward second breakdown due to lateral instability in power transistors operating at low frequency. The method of analysis is to derive the steady-state current density and temperature distribution of a given transistor design under specified operating conditions and then calculate the response of the device to an intervally applied temperature impulse. The current flow calculations have been carried out using a distributed transistor model and a finite difference approach is used for the time-dependent heat flow problem. The effect of device design parameters such as chip thickness, base width, emitter width, base impurity concentration, etc., on the thermal stability has been calculated. Also the effect on transistor stability of the current and voltage operating point, as well as heat sink temperature has been analyzed. Information on the stability of a power transistor under pulsed conditions is derived by calculating the time constant in the case of thermal run away. A simple experimental technique for determining the temperature distribution on the surface of a transistor chip under normal operating conditions using liquid crystals, has been developed. This, coupled with electrical voltage probing, permits an estimation of the current density distribution in the transistor emitter fingers. A test circuit has been constructed for the determination of the power limitation due to second breakdown. DC and pulsed operation as well as the temperature dependence of this failure mechanism have been studied in a preliminary way. Finally, a method for calculating the stabilizing effect of emitter resistor ballasting is indicated and a new technique for improvement of the second breakdown behavior of transistors is proposed. The latter method involves the use of a deposited thin film germanium resistor to sense the temperature locally

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ABSTRACT

A theoretical model has been developed for the prediction of forward bias second breakdown due to lateral thermal instability in power transistors operating at low frequency. The method of analysis is to derive the steady-state current density and temperature distribution of a given transistor design under specified operating conditions and then calculate the response of the device to an internally applied temperature impulse. The current flow calculations have been carried out using a distributed transistor model and a finite difference approach is used for the time-dependent heat flow problem. The effect of device design parameters such as chip thickness, base width, emitter width, base impurity concentration, etc., on the thermal stability has been calculated. Also the effect on transistor stability of the current and voltage operating point, as well as heat sink temperature has been analyzed. Information on the stability of a power transistor under pulsed conditions is derived by calculating the time constant in the case of thermal run away. A simple experimental technique for determining the temperature distribution on the surface of a transistor chip under normal operating conditions using liquid crystals, has been developed. This, coupled with electrical voltage probing, permits an estimation of the current density distribution in the transistor emitter fingers. A test circuit has been constructed for the determination of the power limitation due to second breakdown. DC and pulsed operation as well as the temperature dependence of this failure mechanism have been studied in a preliminary way.

Finally a method for calculating the stabilizing effect of emitter resistor ballasting is indicated and a new technique for improvement of the forward bias second breakdown behavior of transistors is proposed. The latter method involves the use of a deposited thin film germanium resistor to sense the temperature locally and to shunt to ground excess current which may be drawn spuriously by a particular emitter finger.

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I. INTRODUCTION

The primary purpose of the work described in this interim report is to investigate the factors which limit the maximum thermally stable operating power of bipolar transistors, both theoretically and experimentally. The results suggest practical devices designs which are optimized with respect to the reliable operation of power transistors at low frequencies.

The power handling capability of a transistor operating as a switch or amplifier is seriously limited by the phenomenon called "second breakdown". This effect is believed to result from current concentration somewhere in the device in high power operation, causing severe localized heating. Consequently, the device characteristics are often irreversibly degraded.

Due to this failure mode transistors available today are rather limited in their high power capability compared to multilayer semiconductor switches. For example thyristors are available, at a moderate cost, which will handle several hundred amperes and block a thousand volts in a switching application. However transistor switches which can operate reliably at this power level are unavailable at present, mainly due to the second breakdown failure mode. One major difference between transistors and thyristors is that the current injected by the emitter of a transistor is generally not uniform over the whole emitter area but is constricted to the edges or center of the emitter causing local heating there. This is in contrast to the uniform current emission over the whole cathode area of a thyristor in the conducting state. Hence a substantial portion of this research has been devoted to ascertaining both theoretically and

experimentally the device design factors affecting the distribution of current over the emitter area of a power transistor operating in the active region at low frequency.

Much progress has been made in recent years in obtaining a comprehensive understanding of the basic nature of the instability problem observed in the high power operation of bipolar transistors, referred to as second breakdown. A survey of early studies of this phenomenon can be found in a paper by H. A. Schafft [1]. The bulk of these studies indicate that the nature of this instability is basically thermal in origin, deriving from the large positive temperature coefficient of the transistor emitter current. Power dissipated internally in the device, when put in operation in the active mode, occurs mainly in the collector space-charge layer and is given by the product of collector current and the collector voltage across this region. This results in a thermal flux which is directed back towards the emitter junction, heating it and causing additional current to be injected towards the collector. The process then repeats itself resulting either in the achievement of a steady-state current density and temperature distribution or a potentially destructive thermal run away situation. Also a spurious small temperature inhomogeniety (hot spot) somewhere near the emitter junction can cause a severe localization of current and hence a "lateral" thermal instability which grows exponentially with time [2].

Analysis of this problem is complicated by the fact that the emitter current density is never really uniform over the emitter surface in a transistor operating in the active mode. A transverse voltage drop in

the transistor base region due to base current flow tends to bias the emitter current to the emitter edges. At high power densities non-uniform internal heating will also affect the current density distribution in the emitter. This complex situation has been analyzed in some detail using a distributed transistor model [3]. The calculation provided a rough criterion for thermal stability but ignored thermal interactions occuring under the transistor emitter.

A major purpose of this report is to describe a theoretical technique for demonstrating in a more precise manner, whether a specifically defined transistor structure operating with a given collector current and voltage is thermally stable. Only forward second breakdown will be considered where the transistor is operating in the active mode. The component of base current due to collector leakage is not considered. The results of calculations investigating the stability of a variety of transistor structures will be presented. The method used is to first establish the steady-state current density and temperature distribution over the entire emitter junction of a transistor operating in the active region at a particular power level, according to a distributed transistor model [3]. Then a temperature impulse is assumed somewhere near the emitter at a particular instant in time. The current density and temperature redistribution due to this heat spike is then followed in time with the aid of a computer program. Either the effect of this disturbance will settle down in a finite period of time or an instability will occur resulting in thermal run away. Since the current density and temperature distribution are calculated after each small time interval, this model can provide information about the delay time

for thermal run away. This data is very important in evaluating the transistor's capability in pulsed operation.

A test circuit for experimentally determining the thermally stable power capability of commercially available power transistors operating at low frequency is also herein discussed. The results of such measurements on a few device types are presented. The effect of device design, current and voltage operating point and heat sink temperature have been thus experimentally investigated for ultimate correlation with the theoretical studies.

A technique has been developed to determine simply and inexpensively the temperature and current density distribution in a power transistor in operation. The method involves the coating of the transistor surface with cholesteric liquid crystals which are temperature dependent and assume a particular characteristic color of the temperature of the silicon chip, locally. This permits visible observation of the temperature distribution over the transistor surface. Electrical voltage probing along the transistor emitter fingers[1] coupled with the temperature data allowed the current density values along and among the emitter finger to be calculated.

Methods for minimizing the thermal instability of a given transistor structure were investigated. A technique was derived for calculating the value of ballast resistor which must be placed in series with each emitter finger to insure thermal stability by limiting the current carried by that finger should it become higher in temperature than the other fingers. Also discussed

1. Devices with interdigited emitter structures were investigated.

is a new idea for avoiding thermal run away using a temperature sensitive resistor to shunt to ground excess base current which will tend to be drawn by excess temperature rise at a particular site of an operating transistor.

II. THEORETICAL PREDICTION OF SECOND BREAKDOWN

A. Electrical and Thermal Model:

The device chosen for analysis is a nine-finger interdigited power transistor chip which is shown in cross section in Fig. 1. Since the temperature of the innermost emitter finger tends to be maximum, it is expected that the thermal stability of this finger is most critical and hence this center finger alone is analyzed in detail. Only a two-dimensional model of the transistor cross section is assumed and the non-uniformity of current flow due to any voltage drop or temperature variation along the length of the emitter finger is ignored.

The steady state current density and temperature distribution transversely along the emitter base junction are calculated by using a distributed model [3] of the active base region of the transistor. This temperature dependent transistor model makes use of an isothermal model developed by Schlax [4]. The two dimensional transistor geometry considered is shown in Fig. 2. The longitudinal direction is denoted by x-coordinate and the transverse direction is denoted by the y-coordinate. In order to calculate the current and potential distributions in the active base region of the PNP device the following basic equations are used:

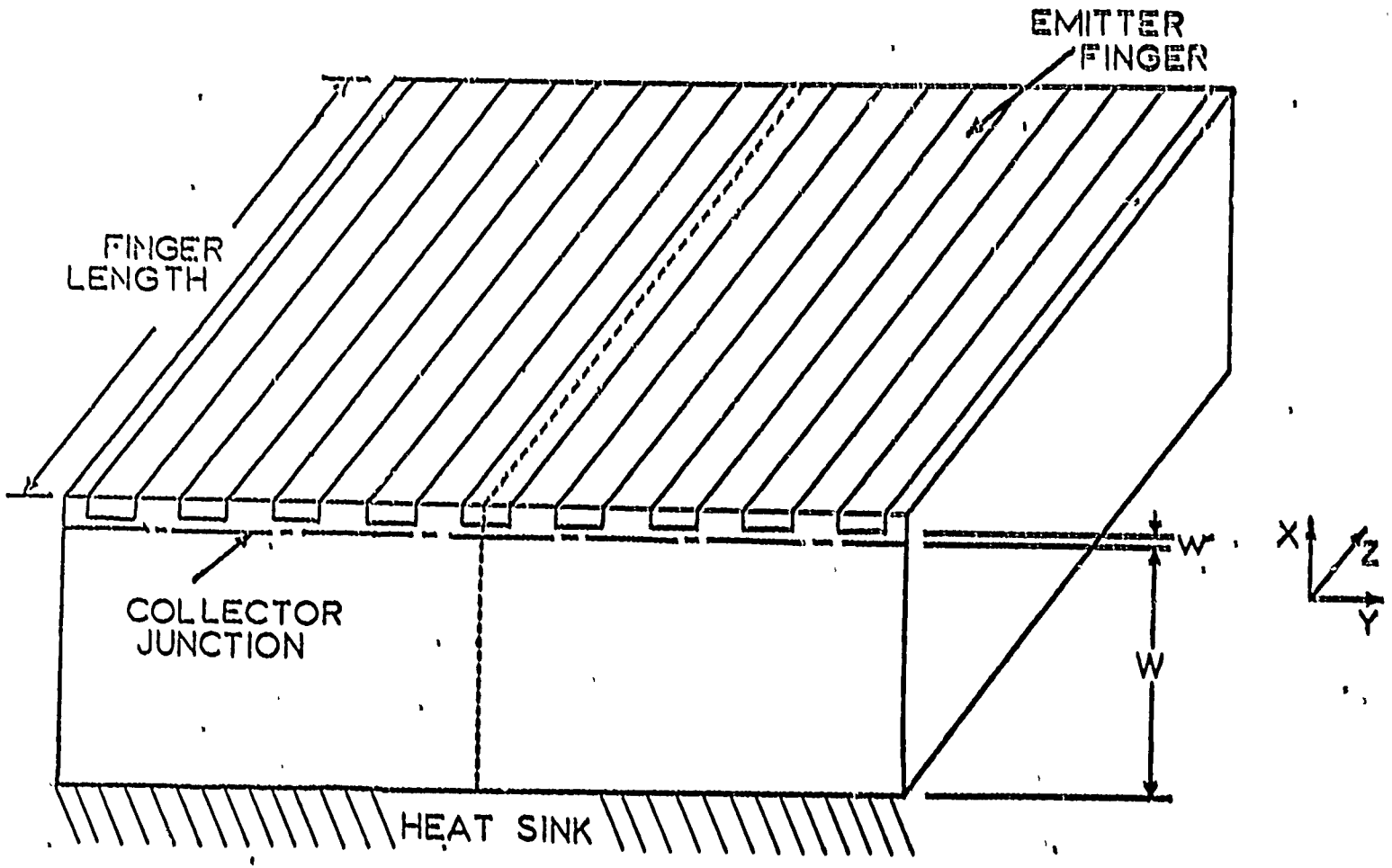


Fig. 1: Multi-emitter interdigited transistor geometry assumed for thermal stability calculations.

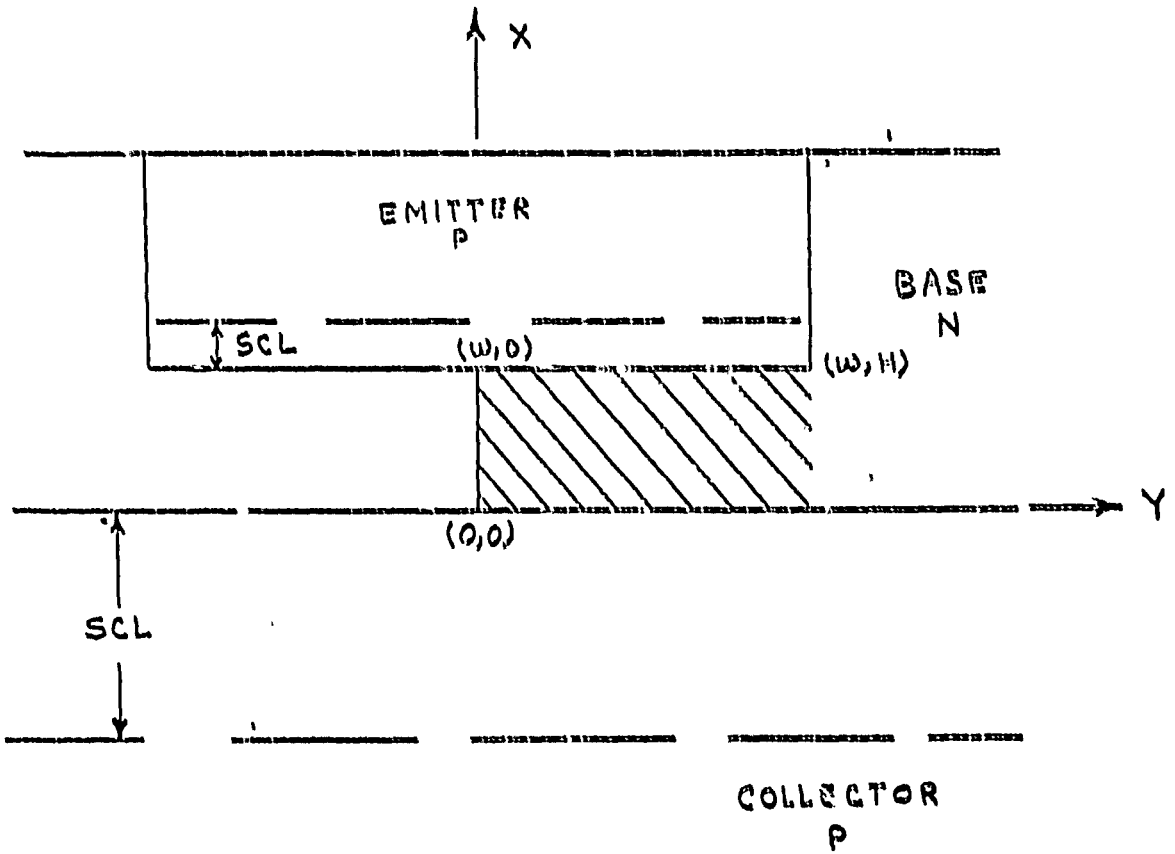


Fig. 2: Structure in which flow is two dimensional.

X - Longitudinal direction

Y - Transverse direction

The flow relations*

$$\vec{J}_p = q\mu_p p\vec{E} - qD_p\vec{\nabla}p \tag{1}$$

$$\vec{J}_e = q\mu_e n\vec{E} + qD_e\vec{\nabla}n \tag{2}$$

The Continuity relationships (assuming no trapping)

$$\frac{1}{q}\vec{\nabla}\cdot\vec{J}_p + \frac{p'}{\tau_p} = 0 \tag{3}$$

$$-\frac{1}{q}\vec{\nabla}\cdot\vec{J}_e + \frac{p'}{\tau_p} = 0 \tag{4}$$

Gauss's Law

$$\vec{\nabla}\cdot\vec{E} = \frac{\rho'}{\epsilon} \tag{5}$$

Maxwell's Equations

$$\vec{\nabla} \times \vec{E} = 0 \tag{6}$$

Steady state conditions and the absence of non-equilibrium volume carrier generation processes are assumed by equations 3,4, and 6.

The distributed model of the transistor consists of a number of one-dimensional transistors with their bases connected through discrete resistors and with their emitters and collectors connected together as shown in Fig. 3. For the present analysis the active base region of a PNP device is broken into forty increments of equal width which corresponds to forty-one parallel transistors.

Because of the non-linear nature of equations 1 - 6 at medium and high levels of injection the following simplifying approximations and

*See page 25ff for definition of symbols used.

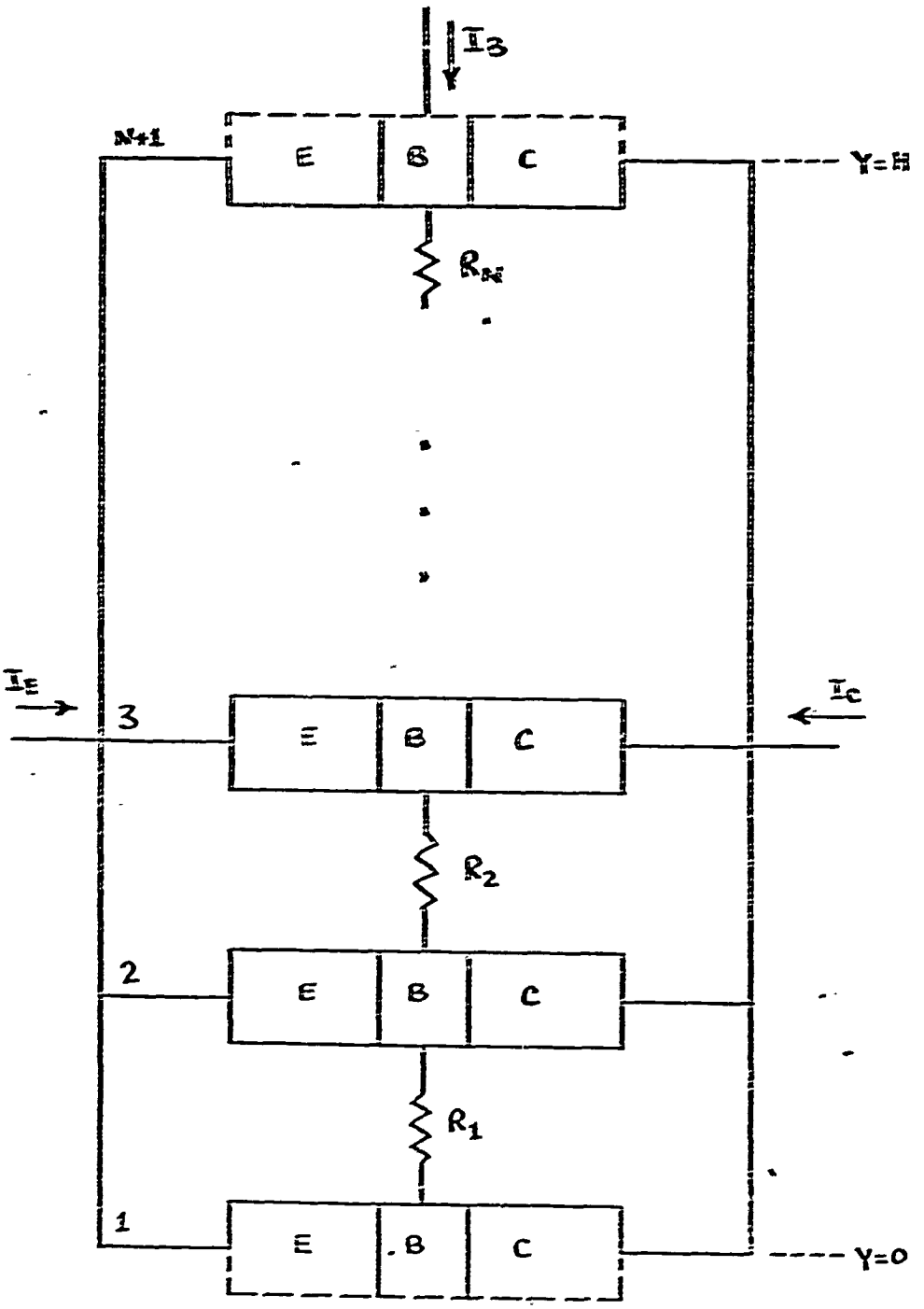


Fig. 3: A Distributed Transistor Model

assumptions are made:

(1) The Boltzmann relationship is assumed to hold true along the base emitter junction at all injection levels.

(2) The Einstein relationship is assumed to be true everywhere in the active base region and emitter region.

(3) Quasi-neutrality is assumed to hold true at all injection levels.

(4) It is assumed that there is a linear gradient of minority and majority carriers across the base width in each increment of the active base region.

(5) The carrier concentrations along the entire base-collector junction are assumed uniform and equal to the equilibrium carrier concentration in the active base region.

(6) The lifetime of minority carriers in the base and emitter are assumed to be constant for all levels of current.

(7) Recombination in the base-emitter and base-collector space-charge regior is neglected.

(8) The component of base current injected into the collector region is assumed to be negligible in comparison with the total base current.

(9) The doping profile of the transistor structure is assumed to be uniform in the emitter and base regions with an abrupt junction between. The emitter region is assumed to be very heavily doped with respect to the base region and hence essentially equipotential.

(10) As shown in Fig 2, the device being analyzed is symmetric about the base midplane. Therefore only half of the active base region need be analyzed. The transverse base current at the midplane is zero.

(11) The base width is assumed to be fixed and independent of operating conditions.

(12) The transverse minority carrier current in the base is assumed to be zero.

(13) The total longitudinal majority carrier current density is assumed to be much less than either its drift or diffusion component.

By using the assumption that the longitudinal (x-direction) majority carrier current is much less than either its drift or diffusion components, the longitudinal and transverse components of electric field are expressed [4] by

$$E_x(x,y) = -\frac{kT}{q}\frac{\partial}{\partial x}\ln n(x,y) \tag{7}$$

$$E_y(x,y) = \frac{kT}{q}\frac{\partial}{\partial y}\ln n(x,y) + \frac{kT}{q}\frac{d}{dy}\ln\left[\frac{p(w,y)n(w,y)}{p_o(w,y)}\right] \tag{8}$$

where p and n are the minority and majority carrier concentrations and $p_o(w,y)$ is the equilibrium hole concentration on the base side of the base emitter junction which is assumed to be equal to the equilibrium hole concentration in the base region (i.e., $p_o(w,y) = p_o = n_i^2/n_o$). Substitution of the equations (7) and (8) into equations (1) and (2) give the following expressions for the minority and majority carrier current densities in terms of carrier concentration:

$$J_{hx}(x,y) = -qD_h p(x,y)\frac{\partial}{\partial x}\ln[p(x,y)n(x,y)] \tag{9}$$

$$J_{ey}(x,y) = qD_e n(x,y)\left\{\frac{d}{dy}\ln[p(w,y)n(w,y)] - \frac{d}{dy}\ln[p_o(w,y)]\right\} \tag{10}$$

$$J_{ex}(w,y) = \frac{qD_{ee}p(w,y)n(w,y)}{L_{ee}p_{eo}} , \qquad (11)$$

where

L_{ee} is the diffusion length of electrons in emitter region

$[L_{ee} = (D_{ee}\tau_e)^{1/2}]$,

D_{ee} is the diffusion constant of electrons in the emitter region at low levels of injection and

p_{eo} is the equilibrium hole concentration in the emitter region.

The Einstein relation [$D_e/\mu_e = D_h/\mu_h = kT/q$] is assumed valid for non-equilibrium conditions.

The incremental resistors, R_I, which separate the one-dimensional transistors, are determined by assuming a linear distribution of electron concentration across the base and by using the average electron concentration to define the electron conductivity by

$$\sigma_e^I = q\mu_e^I n_{ave}^I , \qquad (12)$$

where

$$n_{ave}^I = 0.5[n(w,I\Delta y) + n_o] \qquad 1 \leq I \leq N \qquad (13)$$

and

$$\Delta y = \frac{H}{N} \qquad (14)$$

Thus, the incremental resistors can be expressed as follows:

$$R_I = \frac{\Delta y}{L_1 w \sigma_e^I} \qquad (15)$$

where

σ_e^I is the average conductivity of the I^{th} increment,

q is the electronic charge

n_{ave}^{I} is the average electron concentration in the I^{th} increment,

n_o is the equilibrium electron concentration in the active base,

μ_e^I the mobility of electrons in I^{th} increment

H is half the emitter finger width,

N is the number of increments of half the active base, chosen to be 20 for the present analysis,

w is the base width

and L_1 is the emitter finger length.

The carrier mobility μ_e^I is assumed to be a junction of n_{ave}^{I}. The following functional relationships given by Smythe [5] are utilized:

$$\mu_h = \frac{\mu_{ho}}{1 + a_h n(x,y)/n_o} \tag{16}$$

and

$$\mu_e = \frac{\mu_{eo}}{1 + a_e n(x,y)/n_o} \tag{17}$$

where

$$a_h = \frac{\mu_{ho}}{1.5 \times 10^{20}} [n_o - p_o] \tag{18}$$

and

$$a_e = a_h \frac{\mu_{eo}}{\mu_{ho}} . \tag{19}$$

μ_{ho} and μ_{eo} are the low level injection hole and electron mobilities respectively and n is the majority carrier concentration. For the present analysis n(x,y) is taken as the average electron concentration in each

increment and is given by Equation 13. By using the Einstein relation $[D_e/\mu_e = D_h/\mu_h = kT/q]$ and Eqs. (16) and (17), similar functional relationships for the electron and hole diffusion constants are obtained.

In order to determine the transverse potential drop in the base region from the emitter center to emitter edge, the incremental voltage drops across the incremental resistors are summed. The base current of each incremental device is assumed to be composed of two components

$$I_b^I = I_{be}^I + I_{br}^I \qquad 2 \leq I \leq 20 \tag{20}$$

$$I_b^I = 0.5(I_{be}^I + I_{br}^I) \text{ for } I = 1,21,$$

where

I_b^I is the total base current of the I^{th} incremental transistor,

I_{be}^I is the portion of I_b^I injected into the emitter region,

I_{br}^I is the portion of I_b^I which recombines with holes in the base region and where I_b^1 and I_b^{21} are divided by two due to symmetry.

The emitter back injection current of electrons for each increment is given by [4]

$$I_{be}^I = L_1 \Delta y \, J_{ex}(w, I\Delta y). \tag{21}$$

After substituting for J_{ex} from Equation (11), the above equation becomes

$$I_{be}^I = \frac{L_1 \Delta y q D_{ee} p(w, I\Delta y) n(w, I\Delta y)}{L_{ee} p_{eo}} \tag{22}$$

The bulk recombination current is calculated by approximating the minority carrier concentration in each increment by a linear distribution as follows:

$$I_{br}^I = \frac{qwL_1 \Delta y p(w, I\Delta y)}{2\tau_h}, \tag{23}$$

where τ_h is the lifetime of holes in the base region.

At low levels of injection the "emitter defect" [6] is defined as

$$\text{DEFECT} = \frac{I_{be}}{I_b}, \tag{24}$$

where I_b is the total base current and I_{be} is the portion injected back into the emitter. The analytical expression for low level defect is given by [4]

$$\text{DEFECT} = \frac{1}{1 + \dfrac{wL_{ee}p_{eo}}{2D_{ee}\tau_h\, n(w,0)}} \tag{25}$$

The total base current contribution for each incremental transistor is given by I_b^I. However, the total current flowing through each incremental resistor is the sum of the base currents contributed by each preceeding devices. Therefore the current flowing in each resistor is expressed as

$$I_{R_{I+1}} = I_{R_I} + I_b^I \qquad 1 \leq I \leq 19 \tag{26}$$

and

$$I_{R_1} = I_b^1. \tag{27}$$

Since the transverse base current is composed of diffusion and drift components, the incremental voltage drop across each incremental resistor is defined as:

$$\Delta V_I = \gamma_{dr}^I\, I_{R_I} R_I \tag{28}$$

where

$$\gamma_{dr}^I \triangleq \frac{J_{ey}^{\text{Drift}}(w, I\Delta y)}{J_{ey}(w, I\Delta y)}. \tag{29}$$

Here γ_{dr}^I is the fraction of the transverse base current that is drift current in I^{th} increment and satisfies the condition

$$0.5 \leq \gamma_{dr}^{I} \leq 1 \tag{30}$$

For low levels of injection $\gamma_{dr} \simeq 1.0$ and for high levels of injection $\gamma_{dr} \simeq 0.5$ [4].

$J_{ey}(w,I\Delta y)$ is the transverse electron current density in each increment and $J_{ey}^{Drift}(w,I\Delta y)$ is the drift component of transverse electron current density.

Using the Boltzmann relationship and knowing the difference in potential between two discrete points along the base-emitter junction and the minority carrier concentration at one point, the minority carrier concentration at the second point is calculated as follows:

$$p(w,(I+1)\Delta y) = C_1 \exp[\frac{qV_{I+1}}{kT_{I+1}}] \tag{31}$$

and

$$p(w,I\Delta y) = C_1 \exp[\frac{qV_I}{kT_I}], \tag{32}$$

where

C_1 is a constant proportional to the reverse saturation current,

V_I is the junction voltage at a discrete point along the base-emitter junction,

and T_I is the temperature (°K) at a discrete point along the base emitter junction.

Assuming the entire transistor to be an isothermal region

$$T_I = T_{I+1} = T$$

and from equations (31) and (32)

$$\frac{p(w,(I+1)\Delta y)}{p(w,I\Delta y)} = \exp[\frac{q\Delta V_{I+1}}{kT}], \tag{33}$$

where

$$\Delta V_{I+1} \triangleq V_{I+1} - V_I.$$

The assumption that the emitter is isothermal is found to be reasonable at high current levels for values of collector voltage approaching zero only, and as the value of the collector voltage V_{CE} is increased, the d.c. heat dissipated in the collector space-charge region causes a transverse thermal gradient along the emitter-base junction [3].

The temperature distribution in the base region is obtained by solving the heat flow problem in the power transistor structure by finite difference method [7]. The two-dimensional region considered for the heat flow problem is shown in Fig. 4 with assumed boundary conditions. Due to symmetry $\partial T(x,0)/\partial y = 0$. It is also assumed that $\partial T(x,L)/\partial y = 0$ half way between the edge of the center emitter and the edge of the adjacent emitter, considering that most of the heat generated goes into the heat sink and very little is radiated from the edges of the chip. The heat sink is assumed to be held at a uniform fixed temperature, T_s. Assuming that the internal heat generated by the transistor occurs mainly at the base collector junction, the boundary condition at this junction is given by $K\partial T(W,y)/\partial x = V_{CE}J_C(y)$ where K is the thermal conductivity of the transistor semiconductor material, V_{CE} is the emitter to collector voltage which is assumed to be nearly entirely across the base collector junction and $J_C(y)$ is the minority carrier current density at the base-collector junction. It is further assumed that negligible heat is radiated or convected from the chip surface to the ambient. Hence $\partial T/\partial x = 0$ at the chip surface between emitters. The temperature dependence of the thermal conductivity of silicon as measured

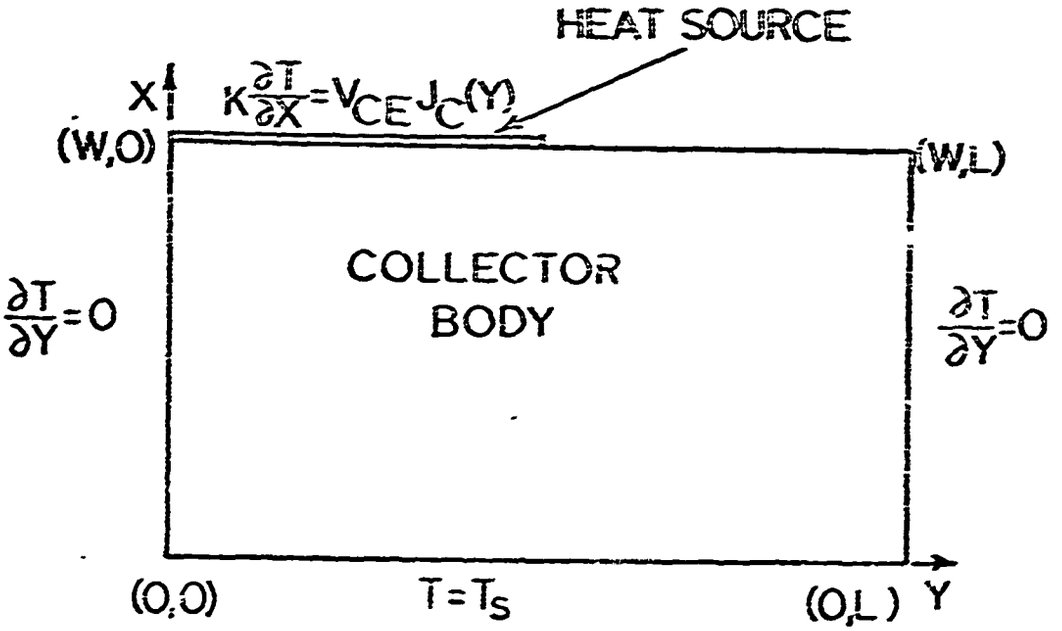


Fig. 4: Region of analysis with assumed boundary conditions for the steady state heat flow problem. Since the temperature of the central emitter finger is maximum, only this finger is considered. Due to symmetry it is necessary to analyze only half of the center finger.

by Glassbrenner and Slack [3] is approximated by the expression

$$K = \frac{3810}{T^{1.35}} \text{ (watts/cm°K)}. \tag{34}$$

The first order computational molecule for the finite difference method of solution of the heat flow problem is shown in Fig. 5. For steady state condition, the heat that enters each node must equal the heat that leaves the node. The heat balance for point (x,y) gives the following expression for the temperature at this node [9]:

$$T(x,y) = \frac{1}{(K_1+K_2+K_3+K_4)} [K_1T(x-h,y)+K_2T(x+h,y)+K_3(x,y-h)+K_4T(x,y+h)], \tag{35}$$

where x and y increments are both taken as h and

K_1 is the thermal conductivity at $\frac{1}{2}[T(x-h,y)+T(x,y)]$,

K_2 is the thermal conductivity at $\frac{1}{2}[T(x+h,y)+T(x,y)]$, etc.

The temperature variation along the emitter-base junction is utilized to calculate the temperature dependence of intrinsic carrier concentration, $n_i(T)$ and the emitter-base junction voltage V_I [5]. The temperature dependence of $n_{i_I}^2$ in the I^{th} increment is expressed as follows [10]:

$$n_{i_I}^2(T) = C_2T_I^3 \exp[-E_{go}/kT_I], \tag{36}$$

where

C_2 is a constant, independent of temperature, and E_{go} is the width of the energy gap extrapolated to absolute zero.

The experimental expression for the intrinsic carrier concentration for silicon is given by [10]

$$n_i(T) = 3.88 \times 10^{16} T^{3/2} e^{-7000/T} \text{ cm}^{-3} \tag{37}$$

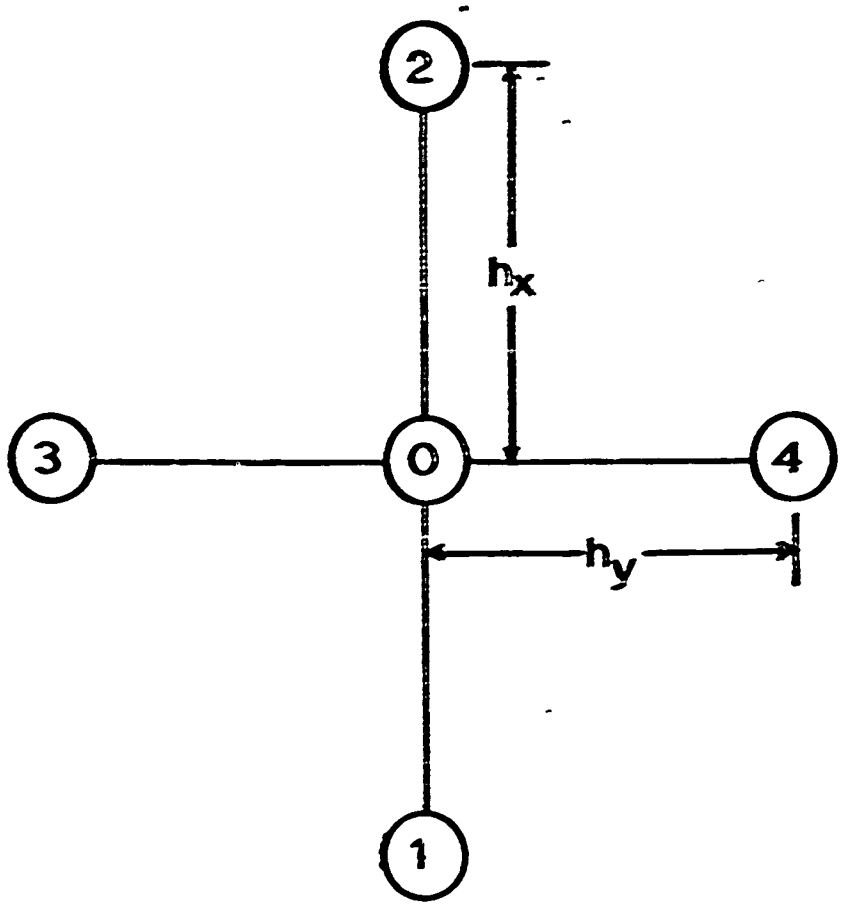


Fig. 5: Typical node for the finite difference method.

As outlined in reference [3] an iterative procedure which modifies the emitter-base voltages is used to obtain a compatible current density and temperature distribution at the emitter-base junction.

The design parameters assumed for the PNP planar transister structure analyzed are listed in Table I. The values of the parameters p_{eo}, τ_e and τ_h are chosen such that the low level defect Eq. (25) is minimized while the value of low level internal gain is held fixed. The analytical expression for the low level internal common emitter gain which is the gain of the active portion of a device, neglecting surface recombination and conductivity modulation in the inactive base region, is as follows [4]:

$$h_{FE} = \frac{2D_n \tau_n}{w^2} \frac{1}{1 + \dfrac{2D_{ee} \tau_n n(w,0)}{w L_{ee} p_{eo}}} \tag{38}$$

By minimizing the low level defect, the percentage crowding that occurs at high levels of injection is minimized and the gain fall off is smaller [4].

The values of low level mobilities μ_{ebo}, μ_{eeo}, μ_{bbo} are obtained by using the data compiled by Irvin [11]. The heat sink temperature is assumed to be 28.5°C unless otherwise specified. The total current density along the emitter-base junction $[J_{nx}(w,y) + J_{ex}(w,y)]$ and the temperature distribution for various design parameters and operating conditions have been calculated and are discussed in the next section.

The stability of a particular operating condition of a specified power transistor design is tested by introducing a temperature impulse somewhere near the emitter junction at a particular instant in time. The current density and temperature redistribution at the emitter-base junction due to

this heat spike is then followed in time with the aid of a computer program. Either the effect of this disturbance will settle down in a finite period of time or an instability will occur resulting in thermal runaway [2].

The region of analysis with assumed boundary conditions for the time-dependent heat flow problem is shown in Fig. 6. Since the assumed symmetry about the base mid plane is no longer valid, the whole base region is analyzed. It should be pointed out that if the heat impulse occurs somewhere between the emitter fingers, the boundary conditions $\partial T(x,L)/\partial y = 0$, and $\partial T(x,-L)/\partial y = 0$ are not very realistic but then the run away situation is less critical. The first order computational molecule for the finite difference method is shown in Fig. 5. For the transient problem the heat that enters each node minus the heat out during a finite time interval must equal the product of the node heat capacity and the node temperature rise during the time interval. Heat balance for the node (x,y) gives the following explicit formulation of the finite difference method [9]:

$$K_1 T(x-h,y,t) - K_2 T(x-h,y,t) + K_3 T(x,y-h,t) + K_4 T(x,y-h,t) - (K_1 + K_2 + K_3 + K_4) T(x,y,t)$$

$$= \frac{\rho c_p h^2}{h_t} [T(x,y,t-h_t) - T(x,y,t)], \qquad (39)$$

where ρ is the mass density, c_p is the specific heat and h_t is the length of the time increment.

After substituting

$$\lambda = \frac{4\rho c_p h^2}{h_t (K_1+K_2+K_3+K_4)} \qquad (40)$$

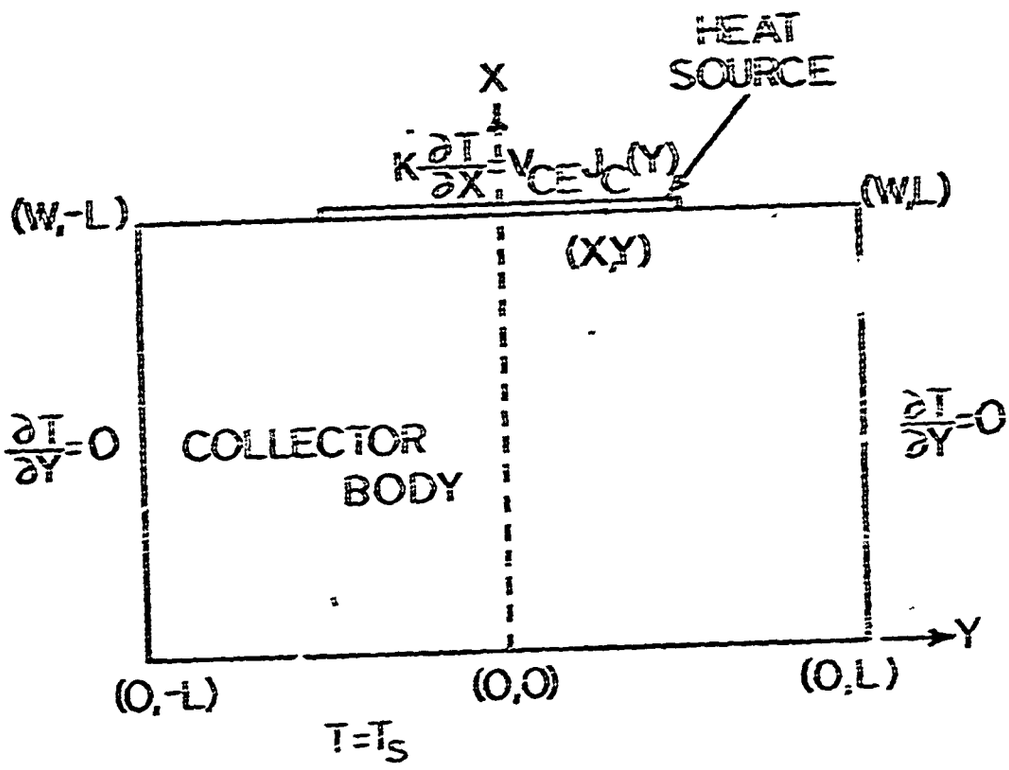


Fig. 6: Region of analysis with assumed boundary conditions for the time-dependent heat flow problem. Only the central emitter is analyzed for thermal stability. A temperature impulse of 3°C is applied at the point (x,y) at time t= 0.

and simplifying, the following expression is obtained for the node temperature as a function of time:

$$T(x,y,t+h_t) = \frac{4}{M(K_1+K_2+K_3+K_4)}\left[K_1T(x-h,y,t)+K_2T(x+h,y,t)\right.$$

$$\left.+K_3T(x,y-h,t)+K_4T(x,y+h,t)\right] + \left(1-\frac{4}{M}\right)T(x,y,t). \quad (41)$$

The value of the spatial interval h is specified and the time interval, h_t, is chosen such that the coefficient $(1-\frac{4}{M})$ in Eq. (41) is always positive. At some particular time instant t = 0, when the transistor is operating in the steady state condition, a temperature impulse of a few degrees centigrade at a point (x,y) somewhere near the emitter, as shown in Fig. 6 is assumed. The corresponding current density redistribution is obtained by the transistor model and the boundary condition $\partial T(W,y)/\partial x = \frac{1}{K} V_{EB} j_C(y)$ in Fig. 6 is correspondingly modified. As an approximation, the values of emitter-base junction voltages, V_{EB}, at the forty-one discrete points are assumed to remain constant at their steady-state values, during this redistribution. Using Equation (41, the temperature distribution after a time interval h_t is obtained and the process again repeated. If the temperature distribution in time settles down to the steady state value, the transistor is said to be operating under stable conditions. On the other hand if the temperature continues to increase, the value of time when the transistor becomes intrinsic is recorded and instability is predicted.

List of Symbols

a_e - constant for the electron mobility variation with concentration

a_h - constant for the hole mobility variation with concentration

C_1 - constant proportional to reverse saturation current

C_2 - constant, independent of temperature, for the temperature variation of intrinsic electron concentration

c_p - specific heat

D_e - Diffusion constant for electrons

D_{ee} - Diffusion constant for electrons in emitter region at low levels of injection

D_h - Diffusion constant for holes

$\vec{E}$ - Electric field

E_{go} - Width of the energy gap extrapolated to absolute zero

h - spatial increment for finite difference method

h_{FE} - internal common emitter gain

h_x - spatial increment in x-direction

h_y - spatial increment in y-direction

h_t - time increment

H - half the emitter width

I_b - base current

I_{be} - portion of base current injected into emitter

I_{br} - portion of base current which recombines with holes in the base region

I_R - current flowing in incremental resistors

$\bar{J}_e$ - electron current density

$\bar{J}_h$ - hole current density

J_c - collector current density

k - Boltzmann constant

K - Thermal conductivity

L - emitter width

L_l - Length of emitter finger

L_{ee} - diffusion length of electrons in emitter region

N - number of increments in half the active base region

n - electron concentration

n_{ave} - the average electron concentration in a incremental transistor base region

n_i - intrinsic electron concentration

n_o - equilibrium electron concentration in the active base region

p - hole concentration

p' - excess hole concentration ($p' = p - p_o$)

p_{eo} - equilibrium hole concentration in emitter

p_o - equilibrium hole concentration in the active base region

q - electron charge

R - incremental resistor

T - temperature

T_s - sink temperature

t - Time

V - Voltage

V_{CE} - Collector to Emitter voltage

V_J - Emitter base junction voltage

w - Base width

W - Collector body thickness

x - longitudinal direction

y - Transverse direction

Δy - width of each increment in the active base region

ρ - Mass density

ρ' - Charge density

σ - Conductivity

ε - Permittivity

γ_{dr} - The fraction of transverse base current that is drift current

τ_h - Hole life time in base region

τ_e - Electron life time in emitter region

μ_e - Mobility of electrons

μ_{eo} - Low level injections electron mobility

μ_{ebo} - Low level electron mobility in base

μ_{eeo} - Low level electron mobility in emitter

μ_h - Hole mobility

μ_{ho} - Low level injection hole mobility

μ_{hbo} - Low level hole mobility in base

B. Calculated Results for Specific Transistor Designs:

A PNP planar power transistor structure with design parameters listed in Table 1 is analyzed. Once the operating conditions are specified the steady-state current density and temperature distribution in the emitter are plotted with the aid of a CalComp plotter. The following design parameters are varied one at a time and the current and temperature distribution at a given power density calculated:

1. Chip thickness
2. Base width
3. Emitter width
4. Base doping

The steady-state current density and temperature distributions have also been calculated for different current and voltage operating points and different heat sink temperatures. These curves are presented in Fig. 7 through 12. Thermal stability is tested in each of these cases by introducing a temperature impulse of 3°C at a point (x,y) shown in Fig. 6 and following the disturbance in time. The results of this test are given on each graph, indicating stable or unstable behavior. In the case of thermal instability, the time constant for thermal run away is indicated.

1. Effect of Varying Collector Current and Voltage for a Given Operating Power Level

The thermal problem encountered in operating a transistor at high voltages at a given power level is indicated in Fig. 7. The central emitter finger of the power transistor, shown in cross section in Fig. 1(a), is taken to be operating at 50 watts dissipation, in the active mode. The current density

Table 1

Design Parameters for a PNP planar Power Transistor Structure

Parameter	Description	Value	Unit
μ_{ebo}	Low level electron mobility in base	1270.0	cm^2/V-sec
μ_{hbo}	Low level hole mobility in base	487.5	cm^2/V-sec
μ_{eeo}	Low level electron mobility in emitter	65.0	cm^2/V-sec
τ_h	Hole lifetime in base region	25	μsec
w	Base width	20.0	μm
p_{eo}	Equilibrium concentration of holes in em	1.5×10^{20}	p/cm^3
n_i	Intrinsic carrier con. at room temp.in Si	1.5×10^{10}	p/cm^3
τ_e	Electron life time in emitter region	2.0	nsec
N	No. of increments in half the base region	20	-
L_1	Emitter finger length	2500.0	μm
n_o	The base doping	1.0×10^{15}	p/cm^3
H	half the finger width	127.0	μm
W	Collector body thickness	3.0	mils

and temperature distribution in half of this emitter is shown in Fig. 7. Note that the peak temperature achieved in the device is about 108°C when operating at 20 Volts and 1.5 Amps., while a maximum temperature of only 62°C is reached at 7.5 volts and 4 amperes; this in spite of the extreme edge "crowding" in the latter case. However the severe crowding in the latter case results in a low grounded-emitter current gain, h_{FE}, of only 3.8. A somewhat reduced current level of 3 amps. gives much less crowding, an h_{FE}

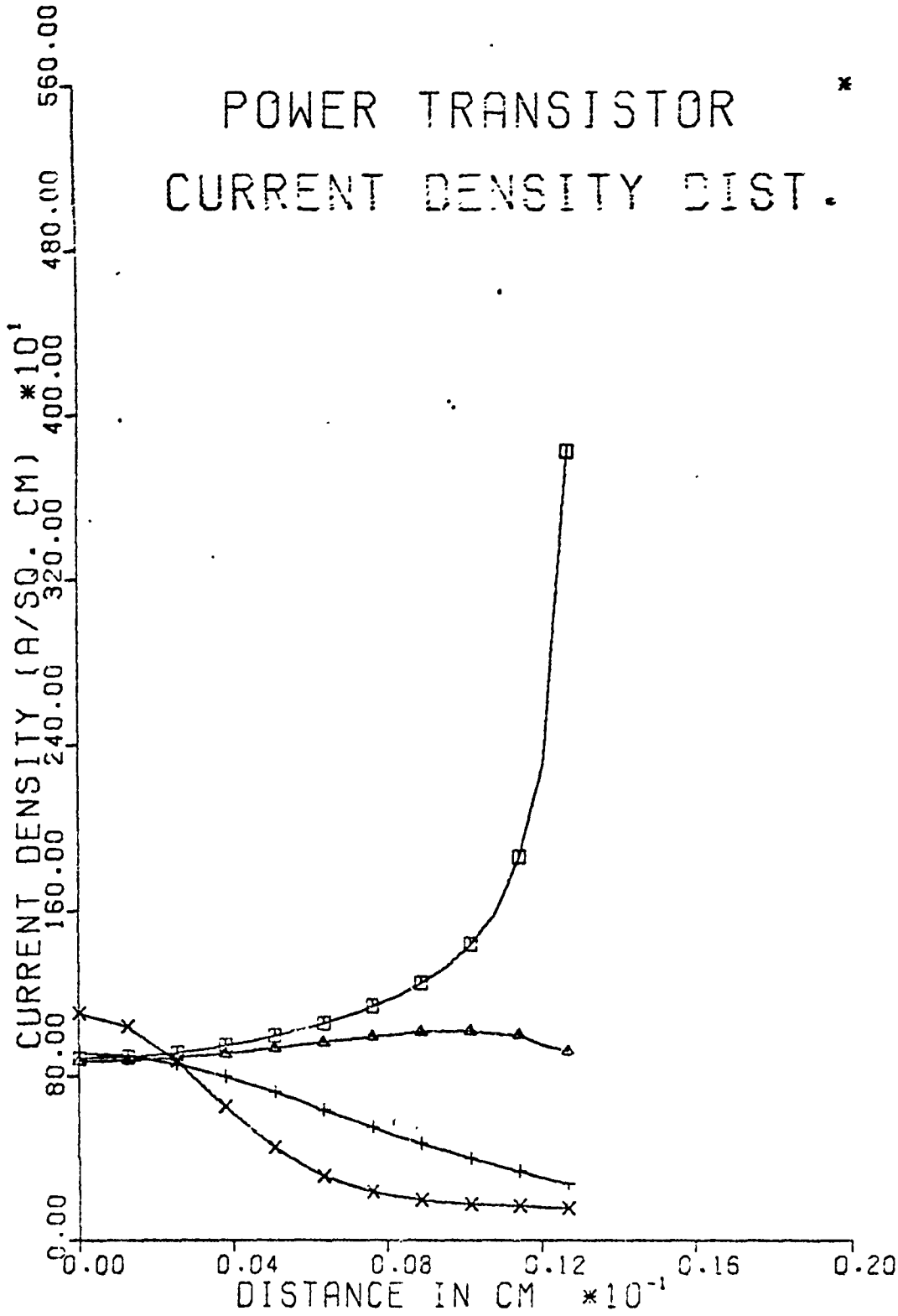

POWER TRANSISTOR
CURRENT DENSITY DIST.
CURRENT DENSITY (A/SQ. CM) *10¹
0.00
80.00
160.00
240.00
320.00
400.00
480.00
560.00
0.00
0.04
0.08
0.12
0.16
0.20
DISTANCE IN CM *10⁻¹

Figure 7A

Fig.7: (a) Current density distributions along half the transistor center finger base emitter junction and (b) temperature distributions along half the central finger width calculated for the following design parameters and operating conditions:

Symbol	X	+	△	□
V_{CE}(volts)	20.0	15.0	10.0	7.5
I_E(amps)	1.5	2.0	3.0	4.0
h_{FE}	36.7	42.4	17.9	3.8
stability	unstable	stable	stable	stable
delay time(ns)	.14	-	-	-

Base Doping = $1 \times 10^{15}/cm^3$

Emitter Doping = $1.5 \times 10^{20}/cm^3$

Base Width = 20 μm

Hole Life Time = 25 μs

Chip thickness = 3 mils (0.00762 cm)

Emitter Width = 10 mils (0.0254 cm)

Sink Temperature = 28.5°C

Emitter Finger Length = 2500 μm

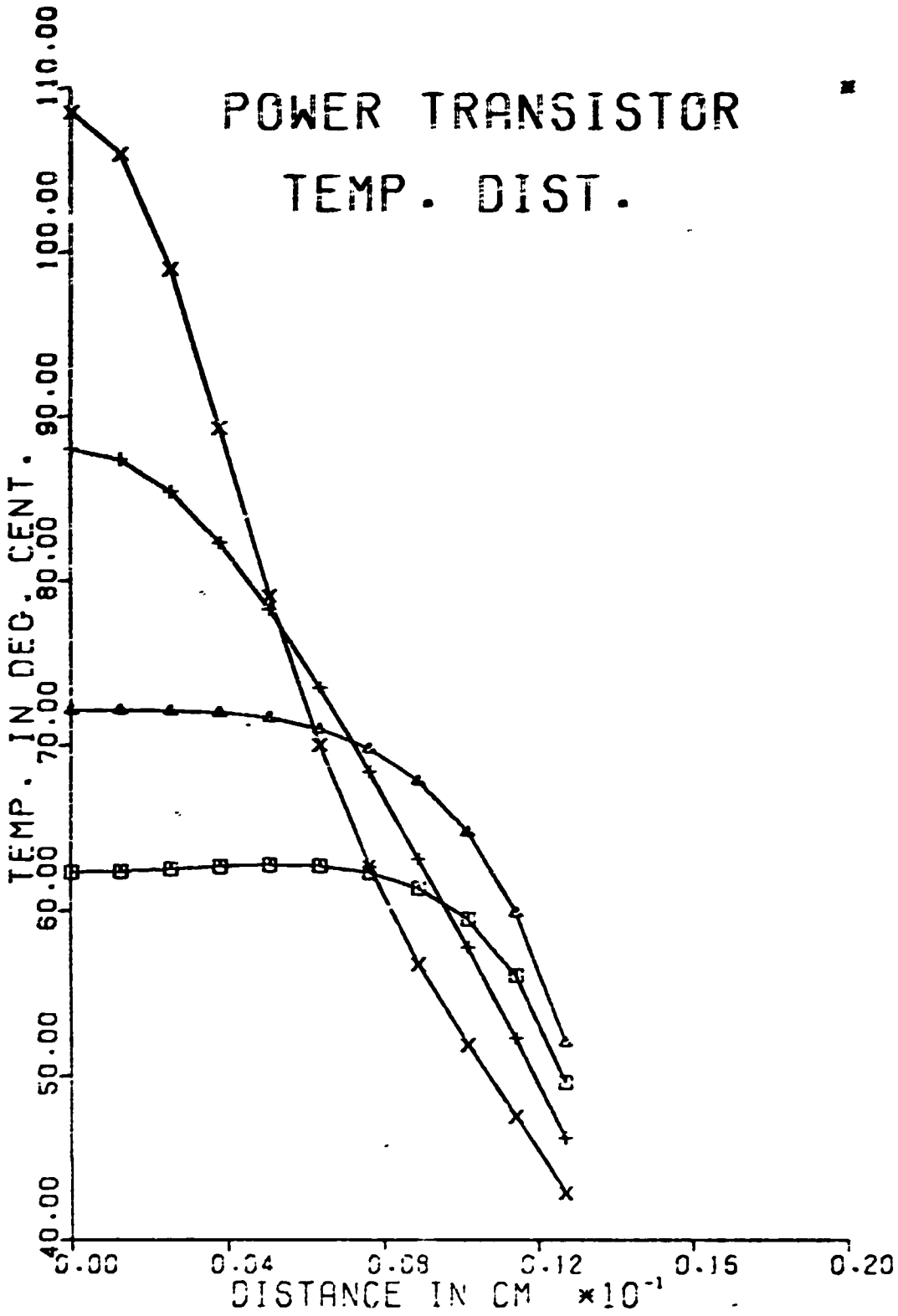

POWER TRANSISTOR
TEMP. DIST.
TEMP. IN DEG. CENT.
110.00
100.00
90.00
80.00
70.00
60.00
50.00
40.00
0.00
0.04
0.08
0.12
0.16
0.20
DISTANCE IN CM ×10⁻¹

Figure 7B

of 17.9, and only a slightly higher temperature maximum.

A stability computation along the lines discussed in Sec. II indicates that the high voltage, low current operating mode is basically unstable while the low voltage, high current cases are thermally stable. This data, presented in Fig. 7, predicts that in the case of instability, a time delay of 0.14 milliseconds occurs before the silicon becomes intrinsic.

2. Effect of Reducing Transistor Chip Thickness

The additional thermal stability achieved by thinning down the transistor chip so that the heat in the device can be more efficiently removed by the heat sink is well known. Fig. 8 however clearly demonstrates quantitatively the reduction in maximum temperature achieved in the transistor emitter, operating at a power level of 60 watts, by reducing the chip thickness from 7 mils to 2 mils. At 7 mils thickness a temperature of 132°C is reached at the emitter center, while the temperature there only reaches 56°C when the chip is thinned to 2 mils. A stability calculation indicates that the device is subject to 2nd breakdown for a chip thickness of 7 mils or more, but is stable for a thickness of 5 mils or less, at 60 watts dissipation. Since the thin chip is essentially isothermal, the transverse base current causes crowding to the emitter edge and hence a somewhat reduced h_{FE} of 13.5. The current gain for each of the four chip thickness considered is indicated in Fig. 8 as well as the time delay in the case of thermal run away which is 0.51 milliseconds.

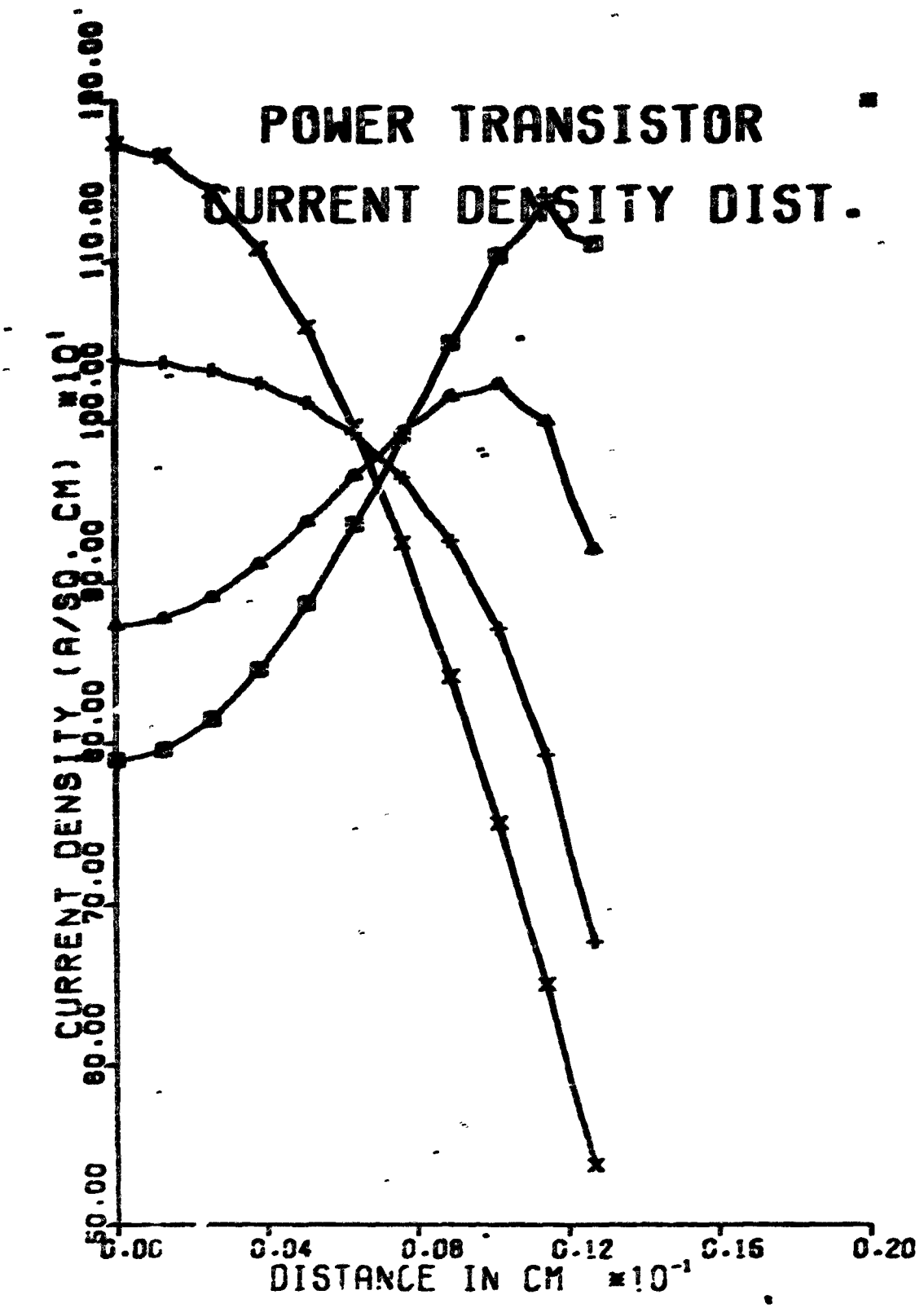

POWER TRANSISTOR
CURRENT DENSITY DIST.
CURRENT DENSITY (A/80.00 CM) *10^1
100.00
110.00
90.00
80.00
70.00
60.00
50.00
0.00
0.04
0.08
0.12
0.16
0.20
DISTANCE IN CM *10^-1

Figure 8A

Fig. 8: (a) Current density distributions along half the transistor center finger base emitter junction and (b) temperature distributions along half the central finger width calculated for the following design parameters and operating conditions:

Symbol	□	Δ	÷	X
Chip Thickness (mils)	2.0	3.0	5.0	7.0
h_{FE}	13.5	17.9	23.3	25.6
Stability	stable	stable	stable	unstable
Delay time(ns)	-	-	-	.51

V_{CE} = 10.0 volts

I_E = 3.0 Amps

Base Doping = 1×10^{15} /cm^3

Emitter Doping = 1.5×10^{20} /cm^3

Base Width = 20 μm

Hole lifetime = 25 μs

Sink Temperature = 28.5°C

Emitter Width = 10 mils (0.0254 cm)

Emitter finger length = 2500 μm

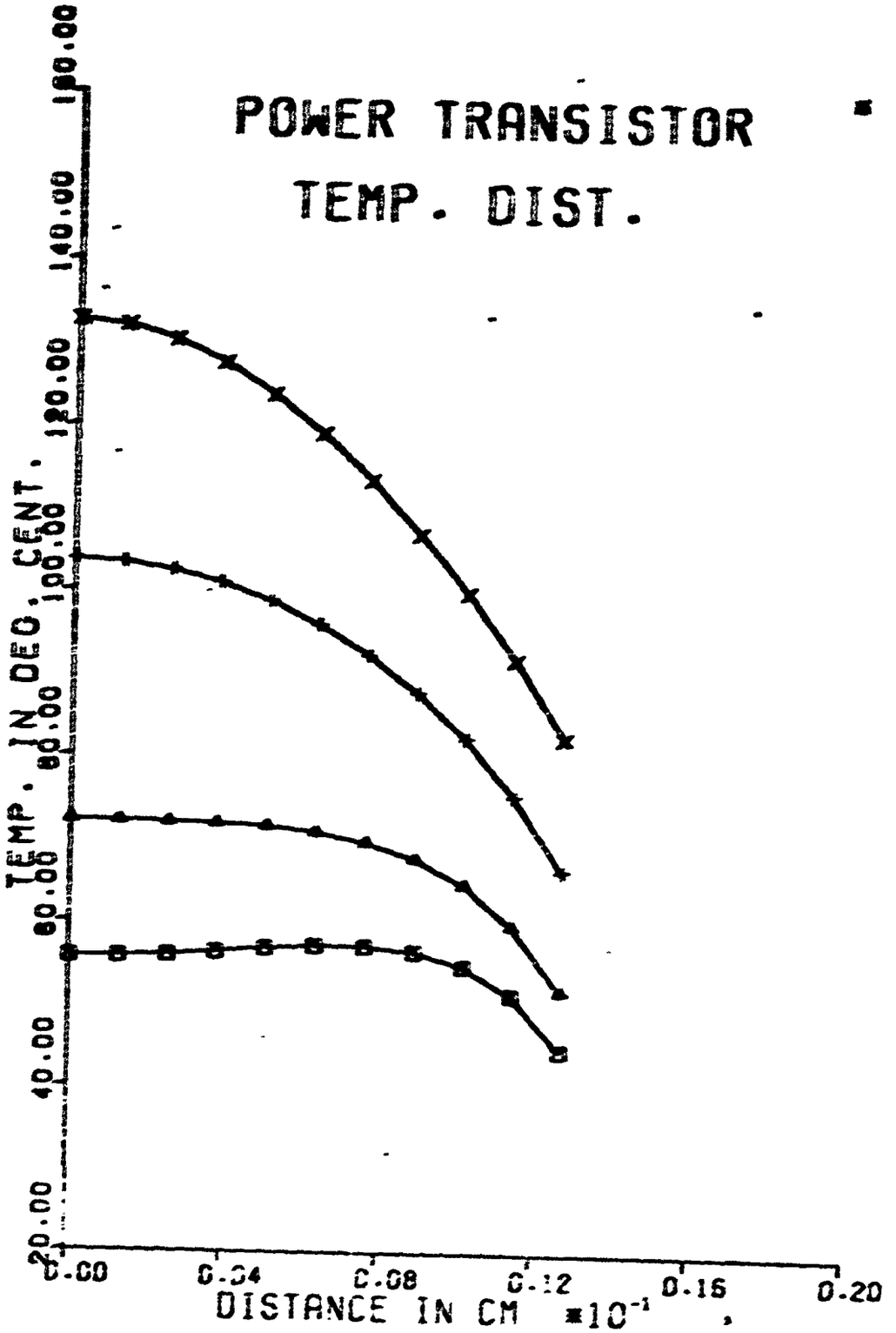

POWER TRANSISTOR
TEMP. DIST.
TEMP. IN DEG. CENT.
180.00
140.00
120.00
100.00
80.00
60.00
40.00
20.00
0.00
0.04
0.08
0.12
0.16
0.20
DISTANCE IN CM *10⁻¹

Figure 8B

3. Effect of Heat Sink Temperature

The possibility of achieving more stable transistor operation by cooling the heat sink is indicated by the results shown in Fig. 9. If the heat sink on which the device is mounted is permitted to rise to a temperature of 100°C or above, while dissipating 60 watts per emitter finger, it becomes thermally unstable and the silicon will become intrinsic 0.33 milliseconds after an initiating heat impulse. This same device nevertheless will operate stably at a heat sink temperature of 65°C or below. Efficient cooling of the heat sink to -25°C will tend to make the chip even more stable and essentially isothermal. But then the transverse base current will cause edge crowding of the emitter current and hence low h_{FE}. These results are shown in Fig. 9.

4. Effects of Base Width Variations

Wide base width power transistors are found experimentally to be more stable thermally than narrow base, potentially high frequency devices when operating at the same power level. This is confirmed by the results of calculations shown in Fig. 10. The current density and temperature distributions are given for devices varying in base from 20 to 5 microns. The lifetime of holes in the base is chosen so as to normalize the current gain in each case to about 15. With the transistor collector operating at 60 watts dissipation, only the 20 and 15 micron base width devices are thermally stable. As the base width is reduced to 10 and 5 microns, thermally unstable operation is predicted and the time constant for thermal run away is reduced as the basewidth is decreased. This is due to severe crowding to the emitter edge caused by the large transverse base voltage drop which results from high base resistance due to the narrow base layer. Note that the current

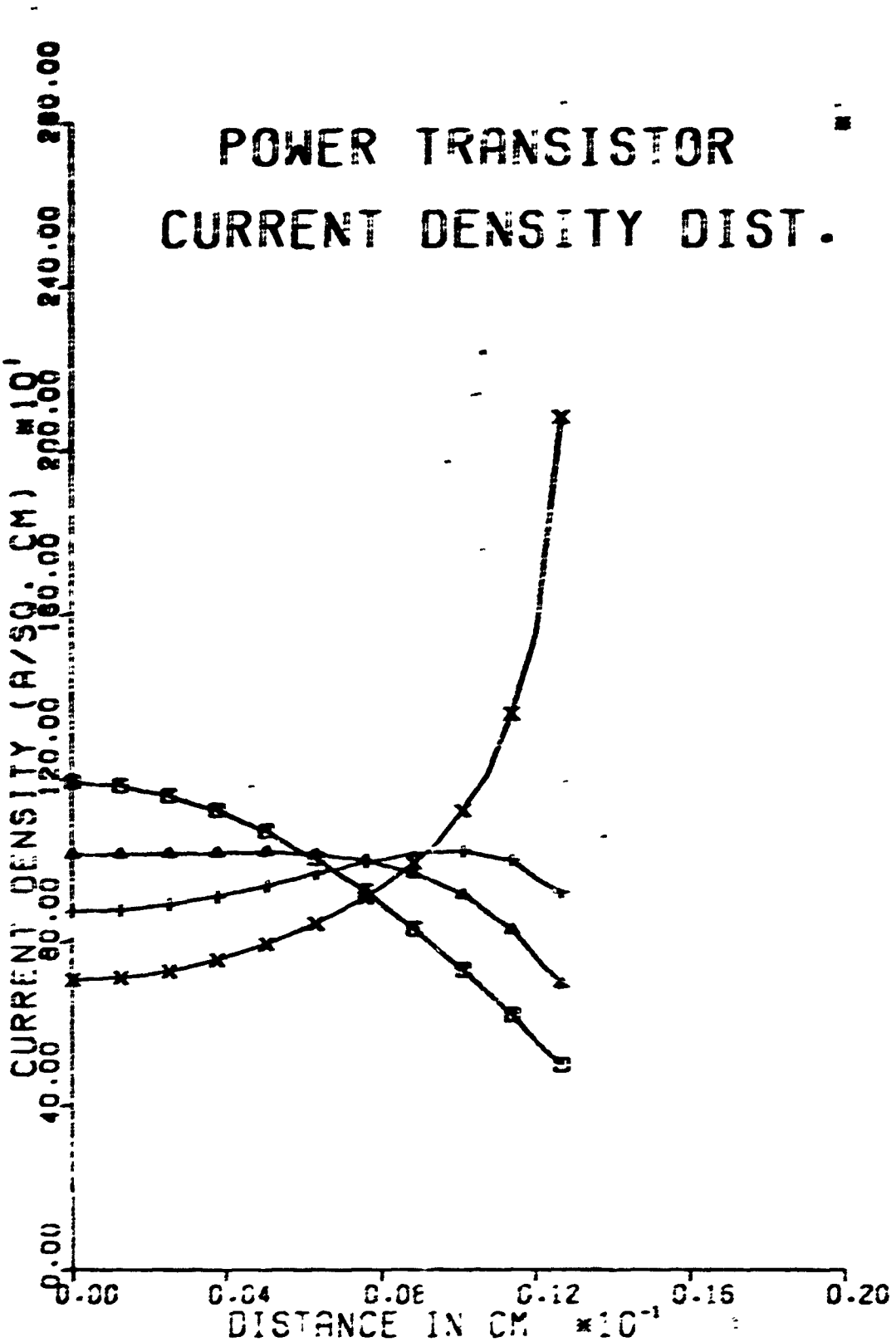

POWER TRANSISTOR
CURRENT DENSITY DIST.
CURRENT DENSITY (A/SQ. CM) *10'
0.00
40.00
80.00
120.00
160.00
200.00
240.00
280.00
0.00
0.04
0.08
0.12
0.16
0.20
DISTANCE IN CM *10⁻¹

Figure 9A

Fig. 9: (a) Current density distributions along half the transistor center finger base emitter junction and (b) temperature distributions along half the central finger width calculated for the following design parameters and operating conditions:

Symbol	□	Δ	+	X
Sink Temp (°C)	100.0	65.0	28.5	-25.0
h_{FE}	35.6	27.8	17.9	5.1
Stability	unstable	stable	stable	stable
Delay time(ns)	.33	-	-	-

V_{CE} = 10.0 volts

I_E = 3.0 Amps

Base Doping = 1×10^{15} /cm^3

Emitter Doping = 1.5×10^{20} /cm^3

Base Width = 20 μm

Hole Lifetime = 25 μs

Chip Thickness = 3 mils (0.00762 cm)

Emitter Width = 10 mils (0.0254 cm)

Emitter finger length = 2500 μm

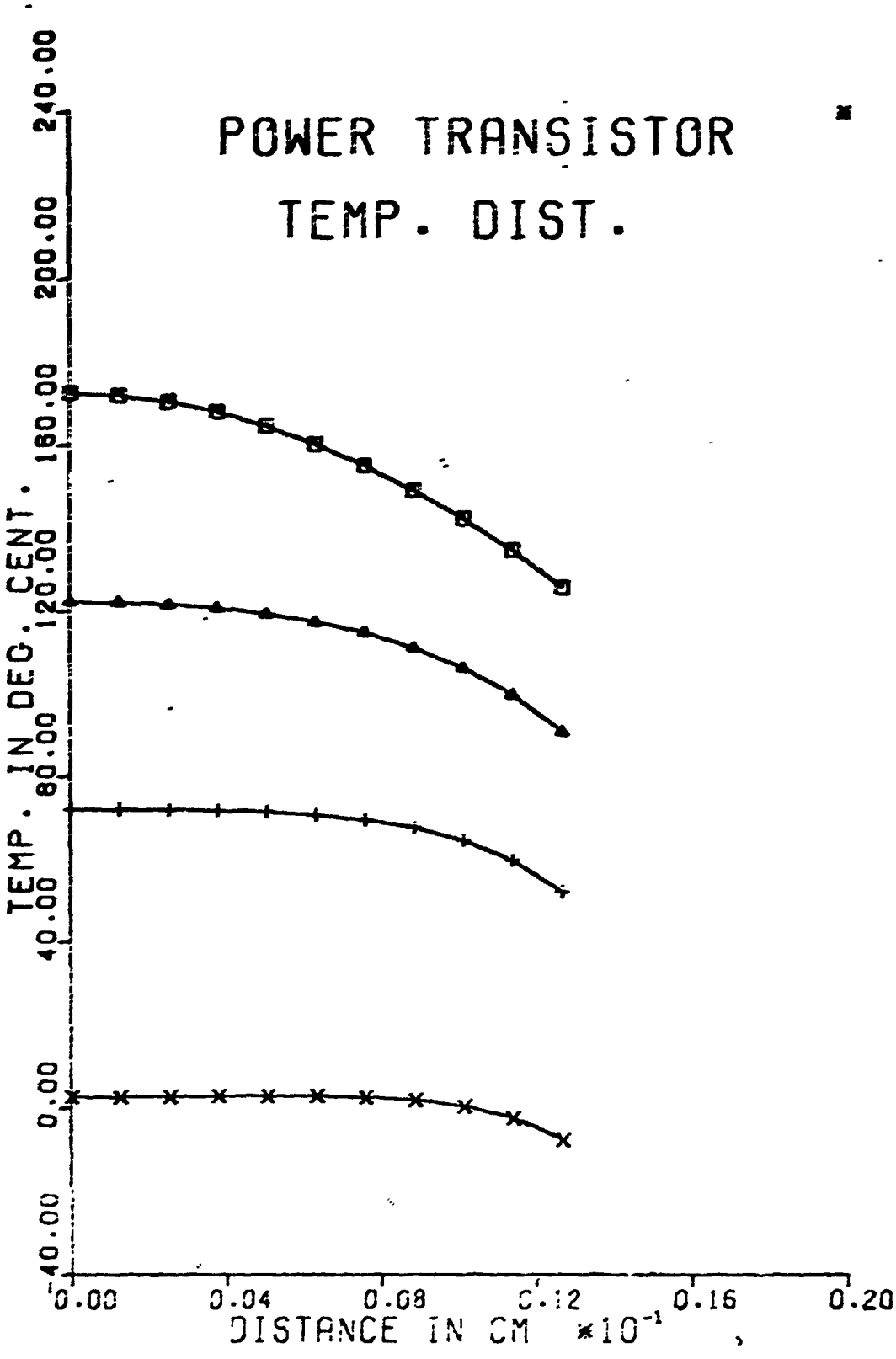

POWER TRANSISTOR
TEMP. DIST.
TEMP. IN DEG. CENT.
240.00
200.00
160.00
120.00
80.00
40.00
0.00
-40.00
0.00
0.04
0.08
0.12
0.16
0.20
DISTANCE IN CM *10^-1

Figure 9B

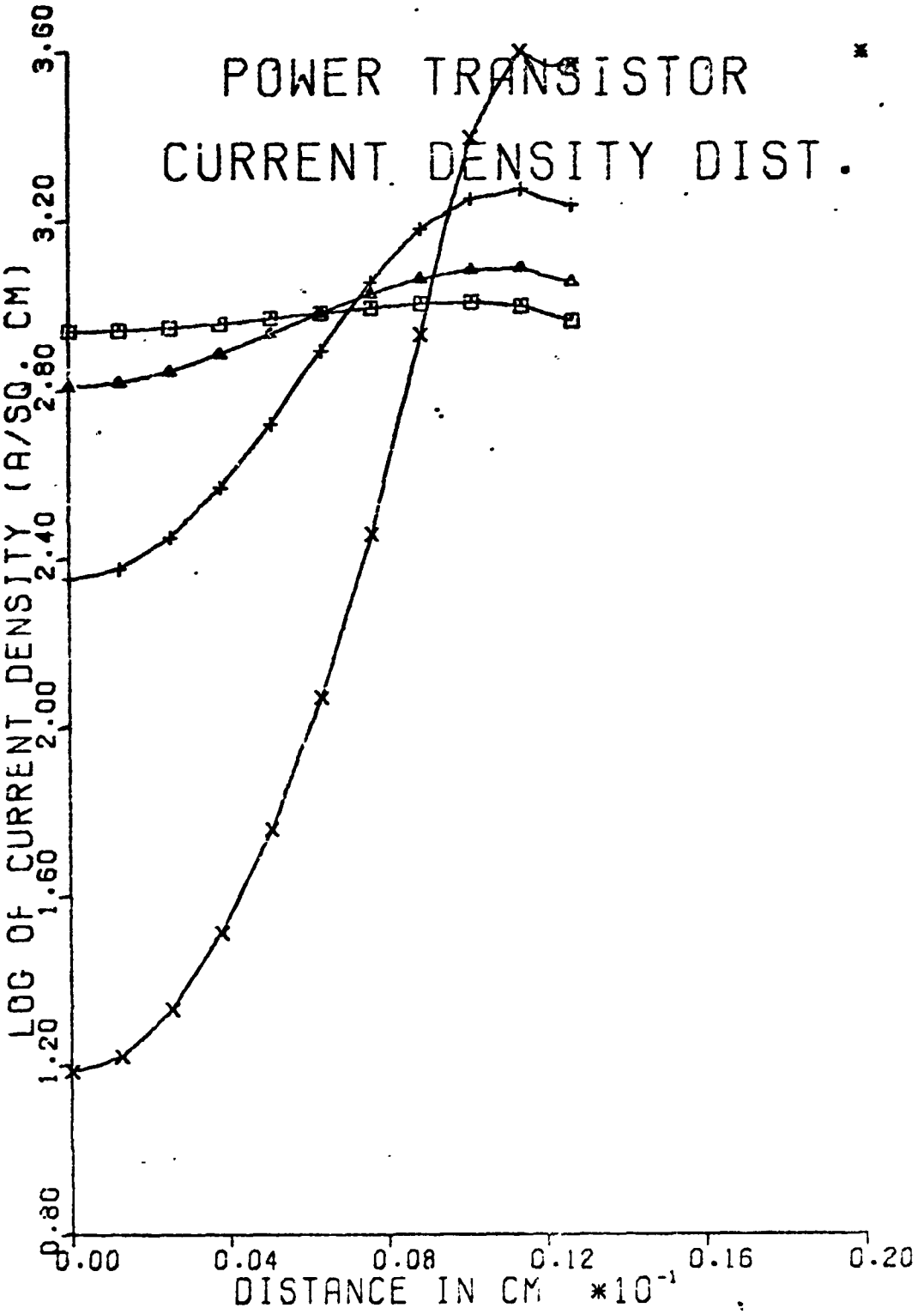

POWER TRANSISTOR
CURRENT DENSITY DIST.
LOG OF CURRENT DENSITY (A/SQ. CM)
3.60
3.20
2.80
2.40
2.00
1.60
1.20
0.80
0.00
0.04
0.08
0.12
0.16
0.20
DISTANCE IN CM *10⁻¹

Figure 10A

Fig.10: (a) Current density distributions along half the transistor center finger base emitter junction and (b) temperature distributions along half the central finger width calculated for the following design parameters and operating conditions:

Symbol	□	Δ	+	×
Base Width(μm)	20.0	15.0	10.0	5.0
Hole Lifetime(μs)	25.0	2.4	.86	.19
h_{FE}	17.9	17.7	18.1	18.2
Stability	stable	stable	unstable	unstable
Delay time(ms)	-	-	.17	.05

V_{CE} = 10.0 volts

I_E = 3.0 amps

Base Doping = 1×10^{15} /cm^3

Emitter Doping = 1.5×10^{20} /cm^3

Chip Thickness = 3 mils (0.00762 cm)

Emitter Width = 10 mils (0.0254 cm)

Sink Temperature = 28.5°C

Emitter Finger Length = 2500 μm

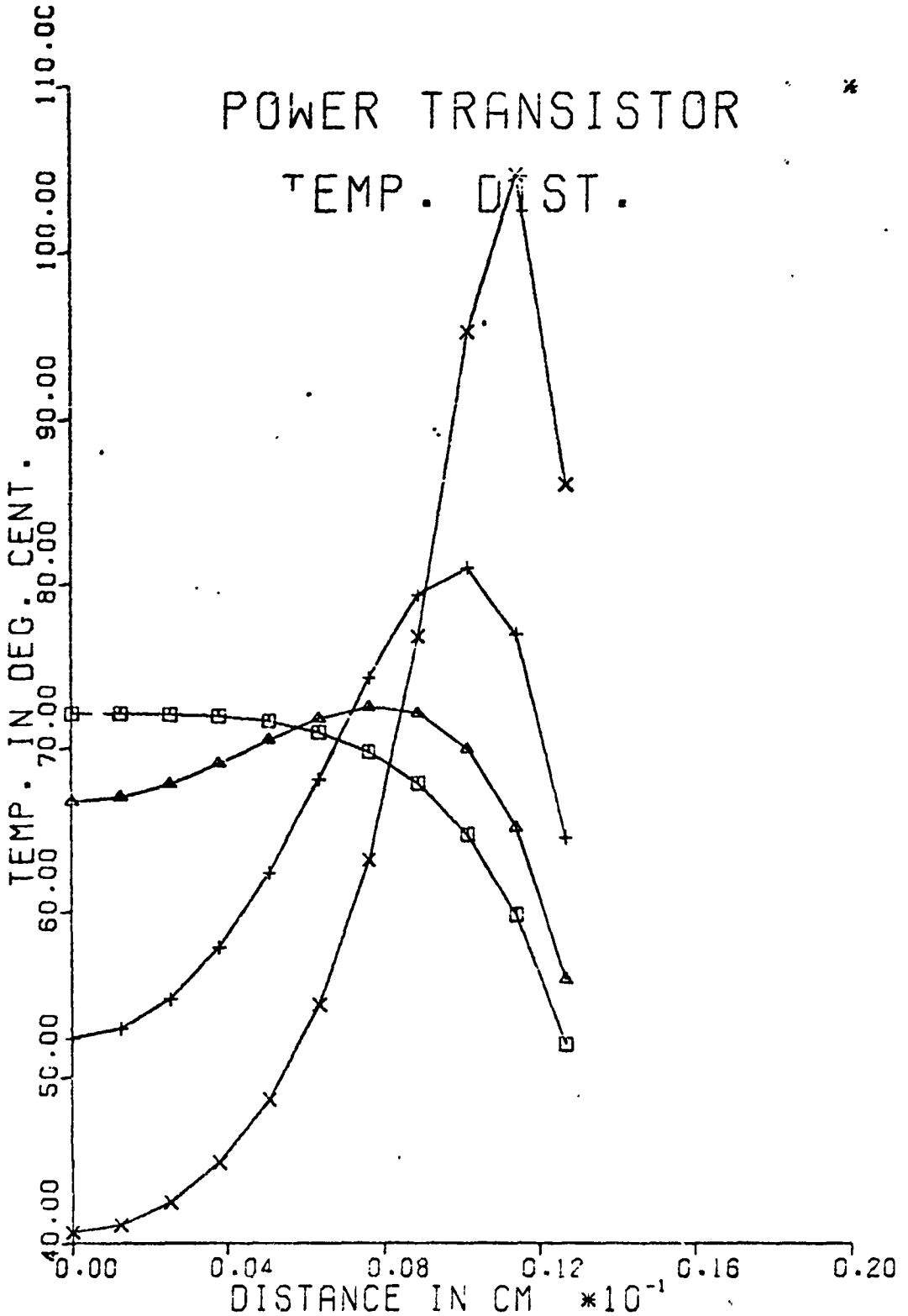

POWER TRANSISTOR
TEMP. DIST.
TEMP. IN DEG. CENT.
110.00
100.00
90.00
80.00
70.00
60.00
50.00
40.00
0.00
0.04
0.08
0.12
0.16
0.20
DISTANCE IN CM *10⁻¹

Figure 10B

density distribution plot of Fig. 10 is semilogarithmic and predicts a current density ratio of more than 1000 to 1 from the emitter edge to the emitter center in the case of the narrowest base layer. These results indicate that other disign or operating power restrictions have to be imposed in order to provide stable narrow base transistor operation. One aid to stable high frequency transistor design is the narrowing of the emitter finger widths. This is demonstrated in Fig. 11.

5. Effect of Varying Emitter Width

Narrowing of the emitter width keeping the same average current density in each emitter, results in more uniform current density and temperature distributions. Also the peak temperature in each emitter finger is reduced as the fingers are narrowed. The wide emitter device tends to exhibit more edge current crowding. Of course a device in which the emitter width has been reduced by a factor of two should have twice as many fingers to be able to compare transistors operating at equal power levels. That is, devices of approximately the same total chip size operating at the same power level, should be compared.

6. Effect of Varying Base Impurity Concentration

It is of interest to consider the effect of increasing the base donor concentration, particularly for narrow base width transistors where the transverse voltage drop due to intrinsic base resistance can cause severe current crowding. The result of varying base doping by four orders of magnitude, from 10^{13} to 10^{17} donor atoms/cm^3 is shown in Fig. 12. Curves are plotted both for the normal base width (20 microns) and for the narrow

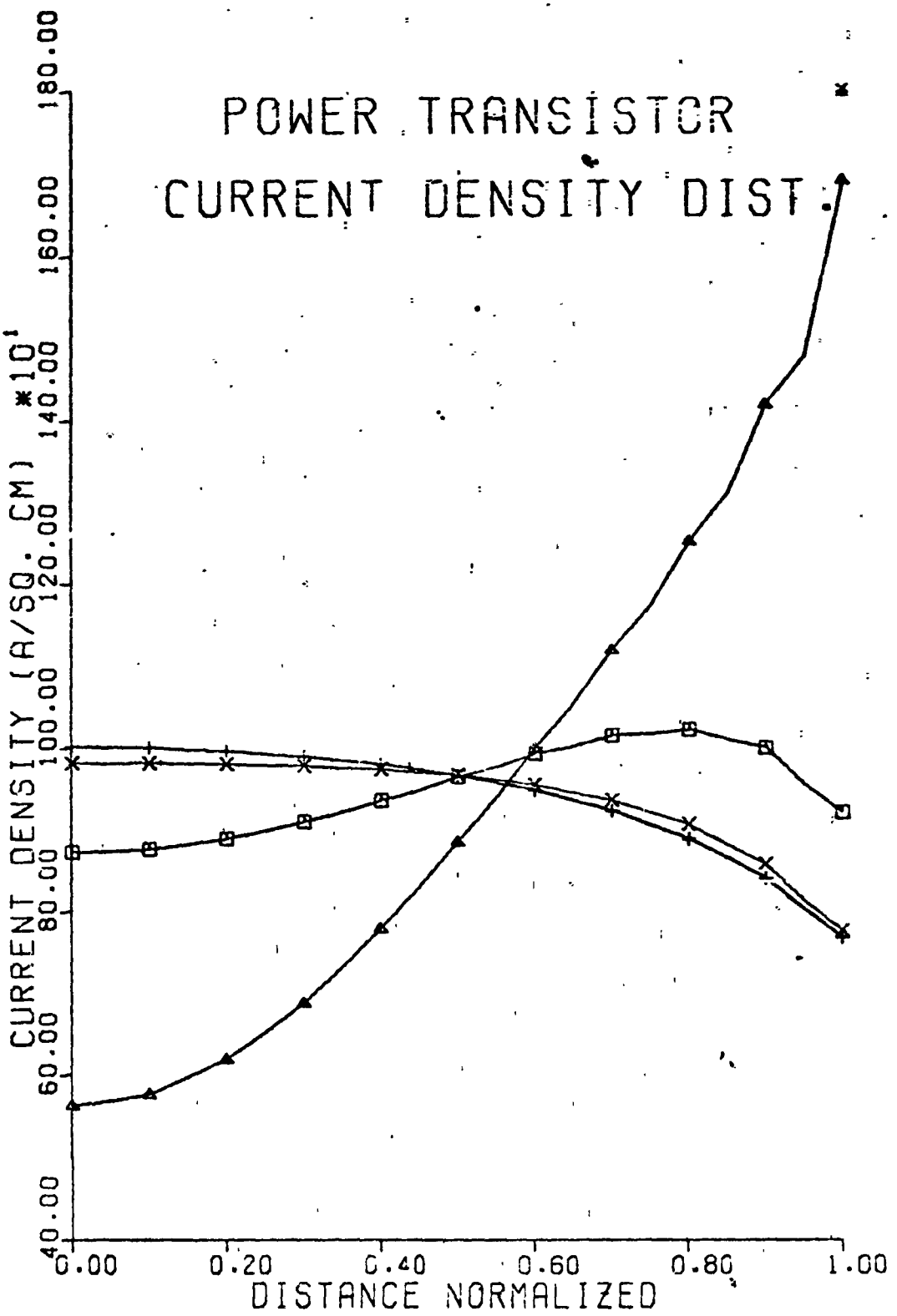

POWER TRANSISTOR
CURRENT DENSITY DIST.
CURRENT DENSITY (A/SQ. CM) *10¹
180.00
160.00
140.00
120.00
100.00
80.00
60.00
40.00
0.00
0.20
0.40
0.60
0.80
1.00
DISTANCE NORMALIZED

Figure 11A

Fig. 11: (a) Current density distributions along half the transistor center finger base emitter junction and (b) temperature distributions along half the central finger width calculated for the following design parameters and operating conditions:

Symbol	Δ	□	X	+
Emitter Width (mils)	15.0	10.0	6.67	5.0
I_E (amps)	4.5	3.0	2.0	1.5
h_{FE}	9.3	17.9	18.2	17.4
Stability	stable	stable	stable	stable

V_{CE} = 10.0 volts

Base Doping = 1×10^{15} /cm^3

Emitter Doping = 1.5×10^{20} /cm^3

Base Width = 20 μm

Hole Lifetime = 25 μs

Chip Thickness = 3 mils (0.00762 cm)

Sink Temperature = 28.5°C

Emitter Finger Length = 2500 μm

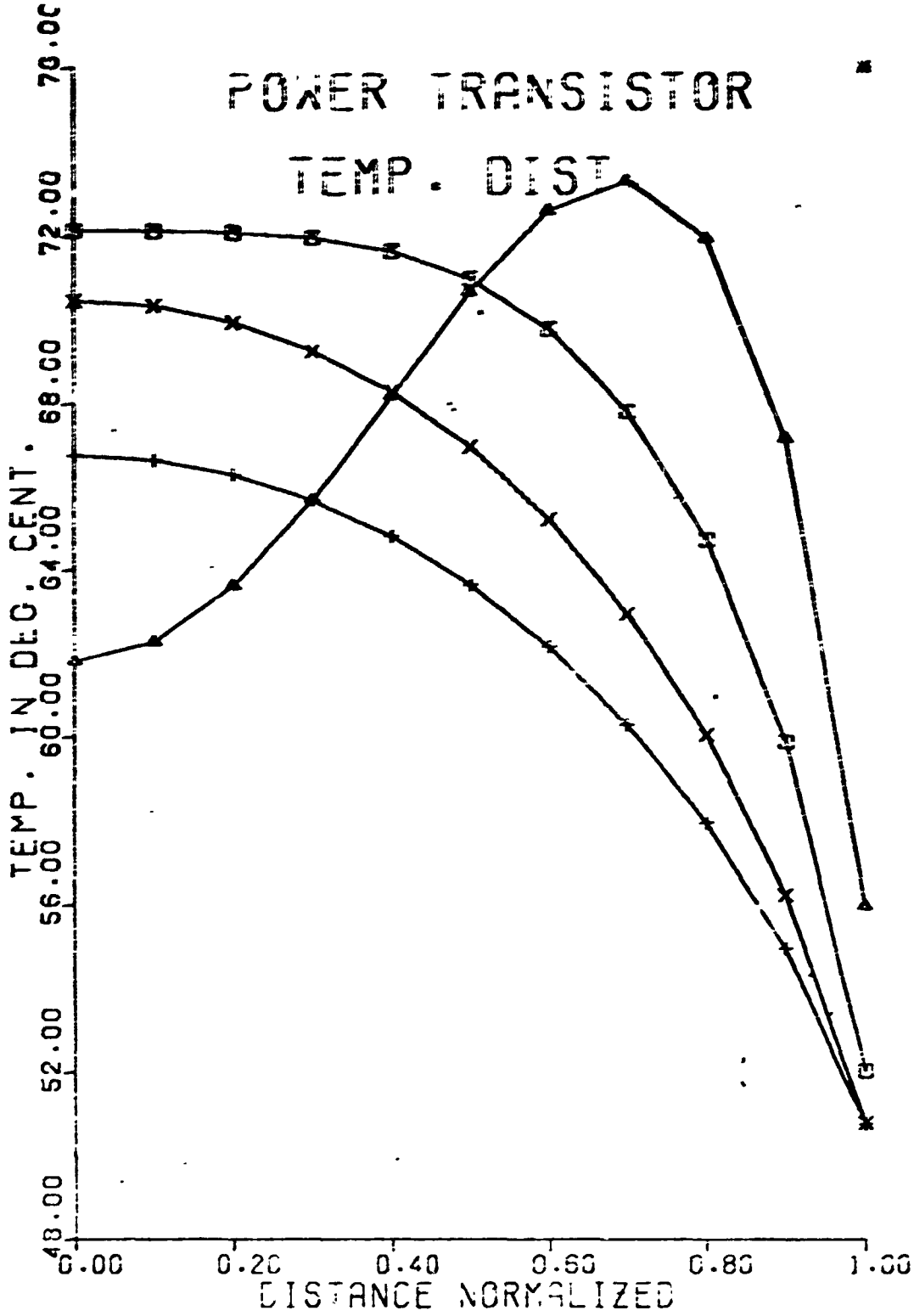

POWER TRANSISTOR
TEMP. DIST
TEMP. IN DEG. CENT.
70.00
72.00
68.00
64.00
60.00
56.00
52.00
48.00
0.00
0.20
0.40
0.60
0.80
1.00
DISTANCE NORMALIZED

Figure 11B

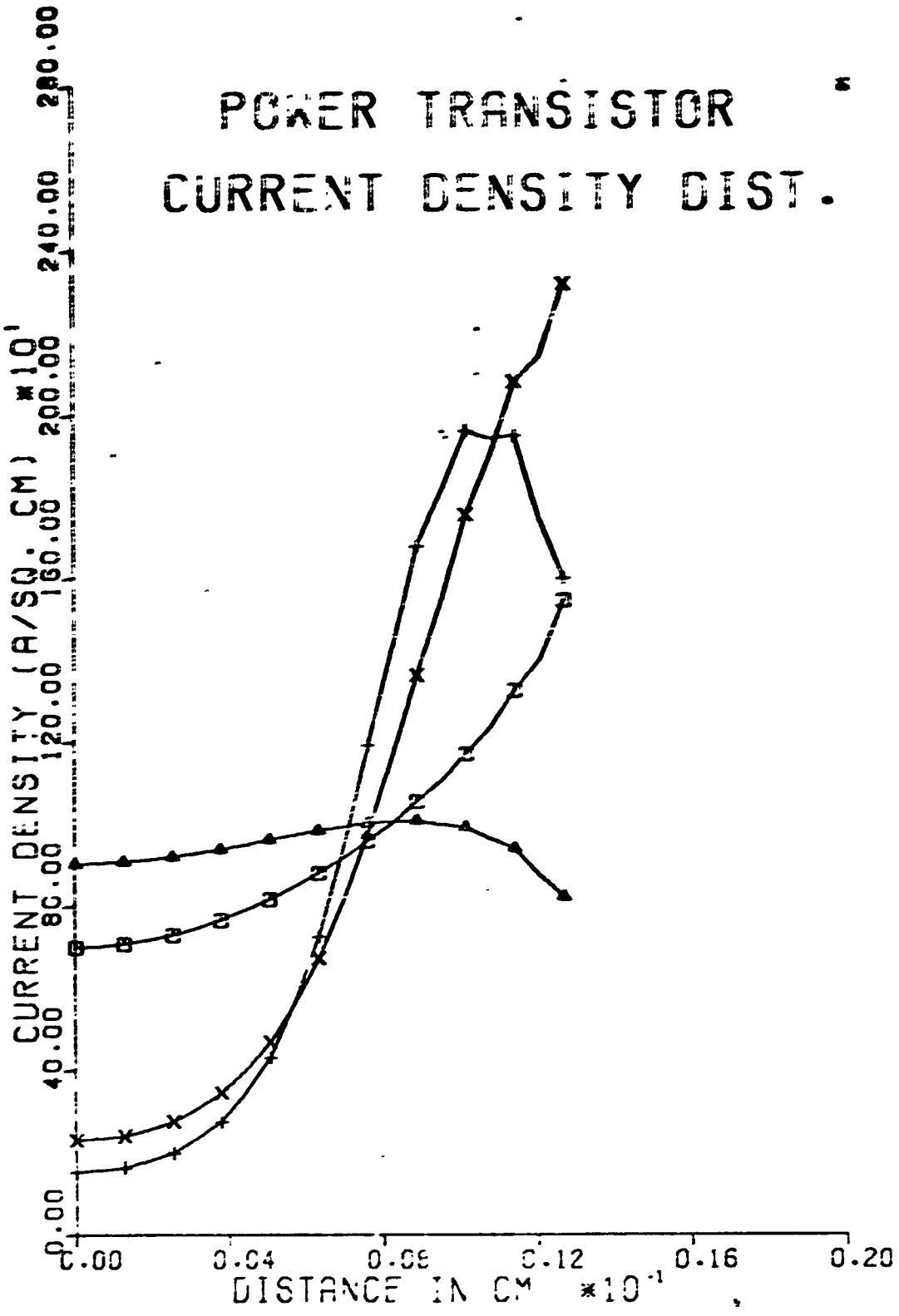

POWER TRANSISTOR
CURRENT DENSITY DIST.
CURRENT DENSITY (A/SQ. CM) *10'
0.00
40.00
80.00
120.00
160.00
200.00
240.00
280.00
0.00
0.04
0.08
0.12
0.16
0.20
DISTANCE IN CM *10⁻¹

Figure 12A

Fig. 11: (a) Current density distributions along half the transistor center finger base emitter junction and (b) temperature distributions along half the central finger width calculated for the following design parameters and operating conditions:

Symbol	○	△	×	+
Base Doping (Atoms/cm^3)	10^{17}	10^{13}	10^{17}	10^{13}
Base Width(μm)	20.0	20.0	10.0	10.0
Hole Lifetime(μs)	25.0	25.0	1.0	1.0
h_{FE}	7.3	18.4	10.2	18.8
Stability	stable	unstable	unstable	unstable
Delay Time(ns)	-	1.44	.47	.07

V_{CE} = 10.0 volts

I_E = 3.0 amps

Emitter Doping = 1.5 x 10^{20} /cm^3

Chip Thickness = 3 mils (0.00762 cm)

Emitter Width = 10 mils (0.0254 cm)

Sink Temperature = 28.5°C

Emitter finger length = 2500 μm

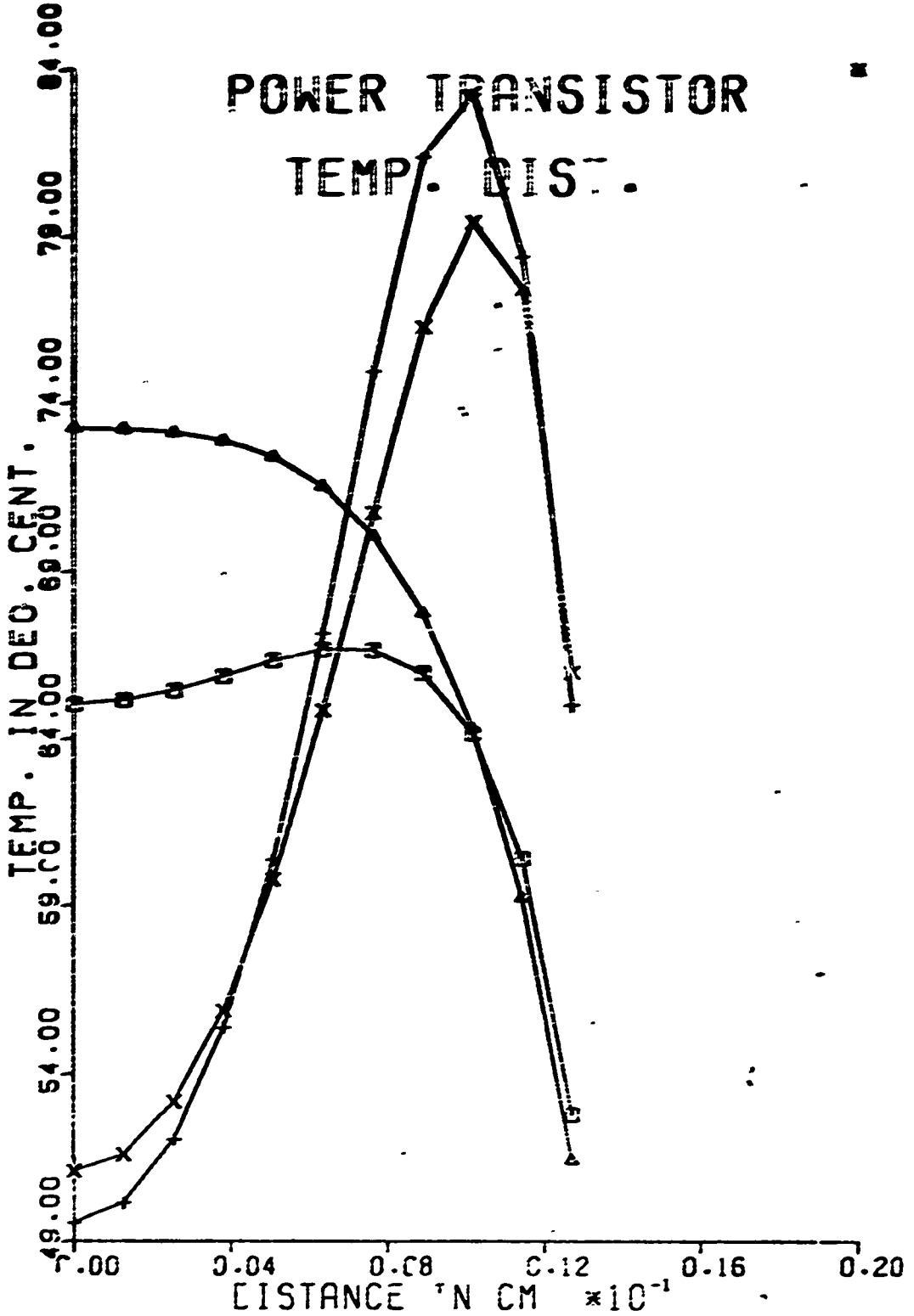

POWER TRANSISTOR
TEMP. DIST.
TEMP. IN DEG. CENT.
49.00
54.00
59.00
64.00
69.00
74.00
79.00
84.00
0.00
0.04
0.08
0.12
0.16
0.20
DISTANCE IN CM *10⁻¹

Figure 12B

base (~0 microns) case. The heavier doping designs generally result in somewhat lower peak temperatures. However the effect is very small, presumably since the base conductivity is severely modulated and the injected carriers essentially determine the base resistance in all cases, rather than the base donor concentration. Note again that the narrow base width results in thermal instability due to severe current crowding to the emitter edge and a high peak temperature there. Again the base lifetimes have been adjusted to tend to normalize the current gains in spite of base width variations. The time constant for thermal runaway appears to be reduced as the base conductivity is decreased.

II. EXPERIMENTAL RESULTS

In order to compare the results of the theoretical calculation of the emitter current density and temperature distribution as well as the stable power limitation of an operating transistor, measurement techniques had to be developed. The current density in a portion of the emitter of a transistor can be calculated if the local emitter-base junction voltage and the temperature are known there. Electrical probing along the emitter fingers was used to determine the longitudinal junction voltage variation. Thermal probing employing cholesteric liquid crystals was used to provide a temperature mapping of the silicon transistor chip surface. Finally a circuit was constructed to stress the transistor to successively higher power levels to the point of 2nd breakdown and then suddenly switching off the power to avoid thermal destruction. In this way the maximum stable operating power for the device was determined.

A. Electrical Probing:

The experimental arrangement for voltage probing along the emitter fingers is sketched in Fig. 13. The sharp steel probes may be placed at different positions along the interdigited emitter and base metallization and the potential at these points determined with respect to the emitter lead potential (taken as zero). Initially a determination was made of the sheet resistance of the emitter and base metallizations. This sheet resistance can be calculated from the formula

$$\text{SHEET RESISTANCE (OHMS/SQUARE)} = \left(\frac{\Delta V}{I}\right)\left(\frac{W}{L}\right), \qquad (42)$$

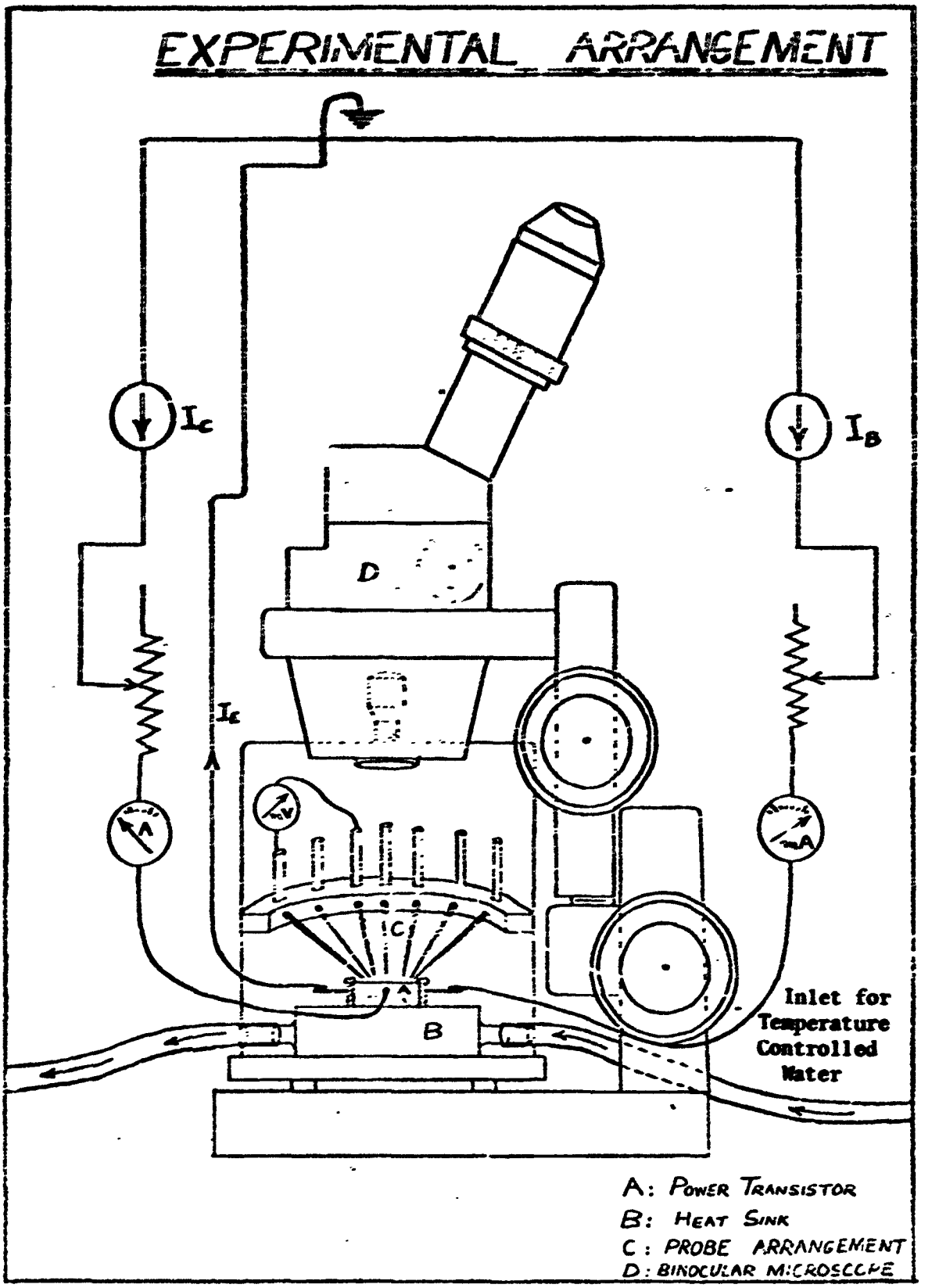

EXPERIMENTAL ARRANGEMENT
I_C
I_B
D
I_E
C
B
Inlet for Temperature Controlled Water
A: Power Transistor
B: Heat Sink
C: Probe Arrangement
D: Binocular Microscope

FIG. 13

where ΔV is the potential difference between two successive points along the metallization spaced a distance L apart. I is the current and W is the width of the metallization. Fig. 14 shows a plot of ΔV in millivolts versus I in amperes for the emitter metallization of an 2N3263 power transistor. The sheet resistance determined from the slope of this curve is found to be 0.0042 Ohms per square for this aluminum metallization.

In an attempt to investigate the uniformity of current emission along the length of an emitter finger, the emitter-base junction voltage was measured at the emitter lead end and at the far end of the finger. If the difference between these voltages (ΔV_1 and ΔV_2 respectively) is negligible, this would indicate uniform emission[3]. However a large discrepancy between these two potential differences would tend to indicate that the emitter current flow is essentially cut off at the far end of the emitter finger. A plot of $(\Delta V_1 - \Delta V_2)$ as a function of total emitter lead current shown in Fig. 15 demonstrates that significant non-uniformity of emitter emission begins to occur at a total emitter current of 5 amps. The initial slope of this curve corresponds to the normal emitter metallization potential drop. The potential drop along the base metallization is negligible over the range of current values used, hence the base metallization may be taken as equipotential.

---

3. The current density at any point along the emitter is assumed to be exponentially dependent on the junction voltage there.

2N3263

SHEET RESISTANCE MEASUREMENTS

ON THE EMITTER FINGER

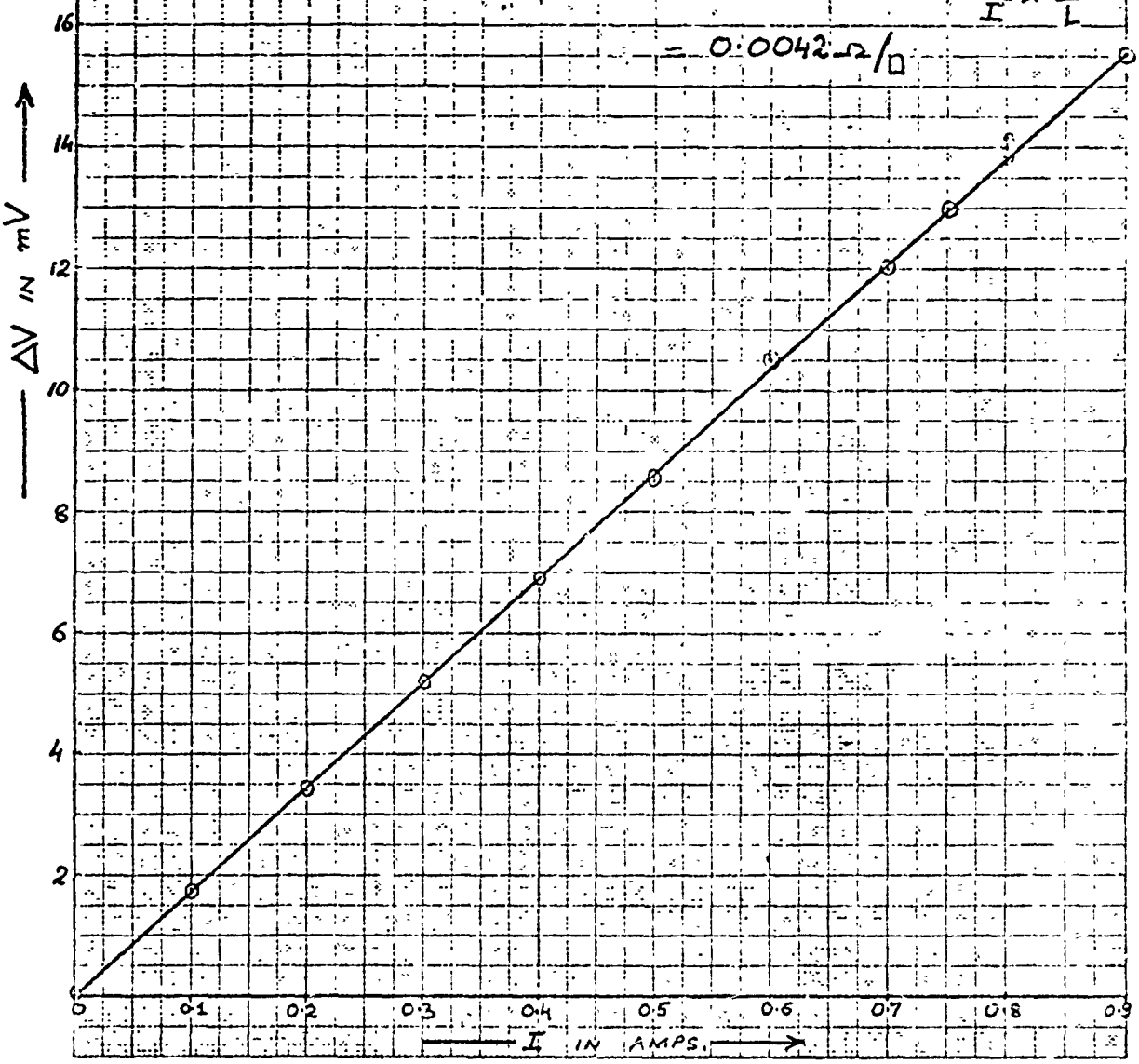
L: PROBE SPACING = 38.0 Mils.

W: EMITTER METALIZATION WIDTH = 9.0 Mils.

SLOPE $\frac{\Delta V}{I} = 1.8 \times 10^{-2}$

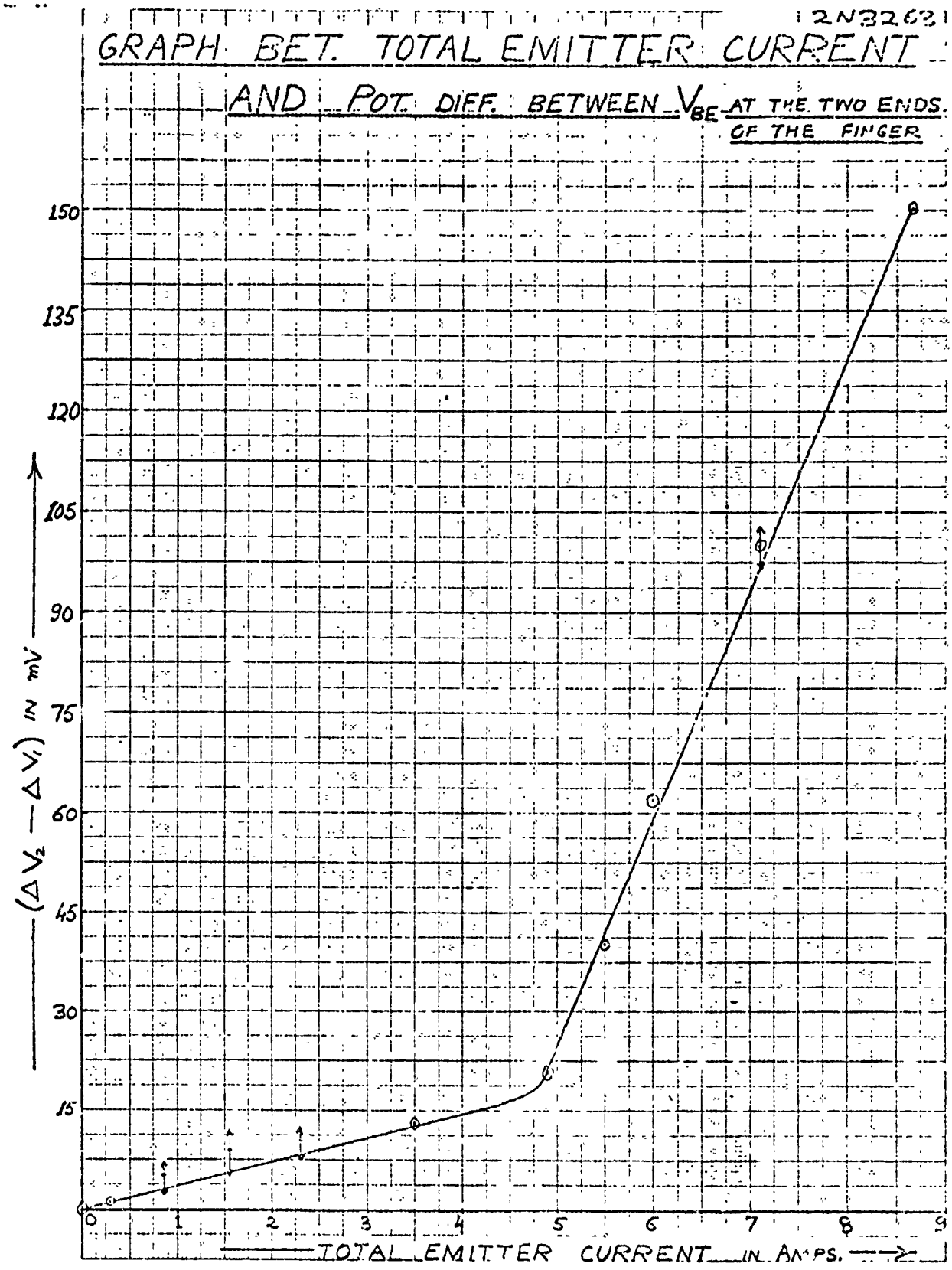
SHEET RESISTANCE = $\frac{\Delta V}{I} \times \frac{W}{L}$

$= 0.0042\ \Omega/\square$



10 Millimeters to the Centimeter

FIG. 14



10 Millimeters to the Centimeter

FIG. 15

It is also of interest to determine whether the outer emitter fingers on the chip carry less current than the central finger at high current levels, since the transistor chip will be cooler at the edges. The result of probe measurements along an outer emitter finger and the central finger are shown in Fig. 15 . The fact that the potential of the central finger is higher than that of the outer finger at all current levels can possibly be explained by the lower temperature at the edges of the chip.

However a true determination of the current density distribution in the transistor chip requires the independent measurement of both voltage and temperature, simultaneously. Then the current density, I_E, can be calculated from the expression

$$I_E = BT^3 \exp\{\frac{-[E_g - q(V_{EB}+I_B R_B)]}{\eta kT}\} , \qquad (43)$$

where T is the absolute temperature, E_g is the energy gap width, q is the electronic charge, V_{EB} is the emitter-base junction voltage, I_B is the base current, R_B the base resistance, k is the Boltzmann constant, η is a number between 1 and 2 and B is a proportionality constant. The conclusions of emitter end cutoff and outer finger cutoff are confirmed by interpreting the data given in Table 2 with the aid of Eq. (43). The voltage difference between the outer and central finger at a collector current of 7.5 Amps. is consistent with an approximate temperature differential of 20°C. However a more precise determination of the current density distribution in the chip requires a separate temperature determination and a method for making this measurement will be described next.

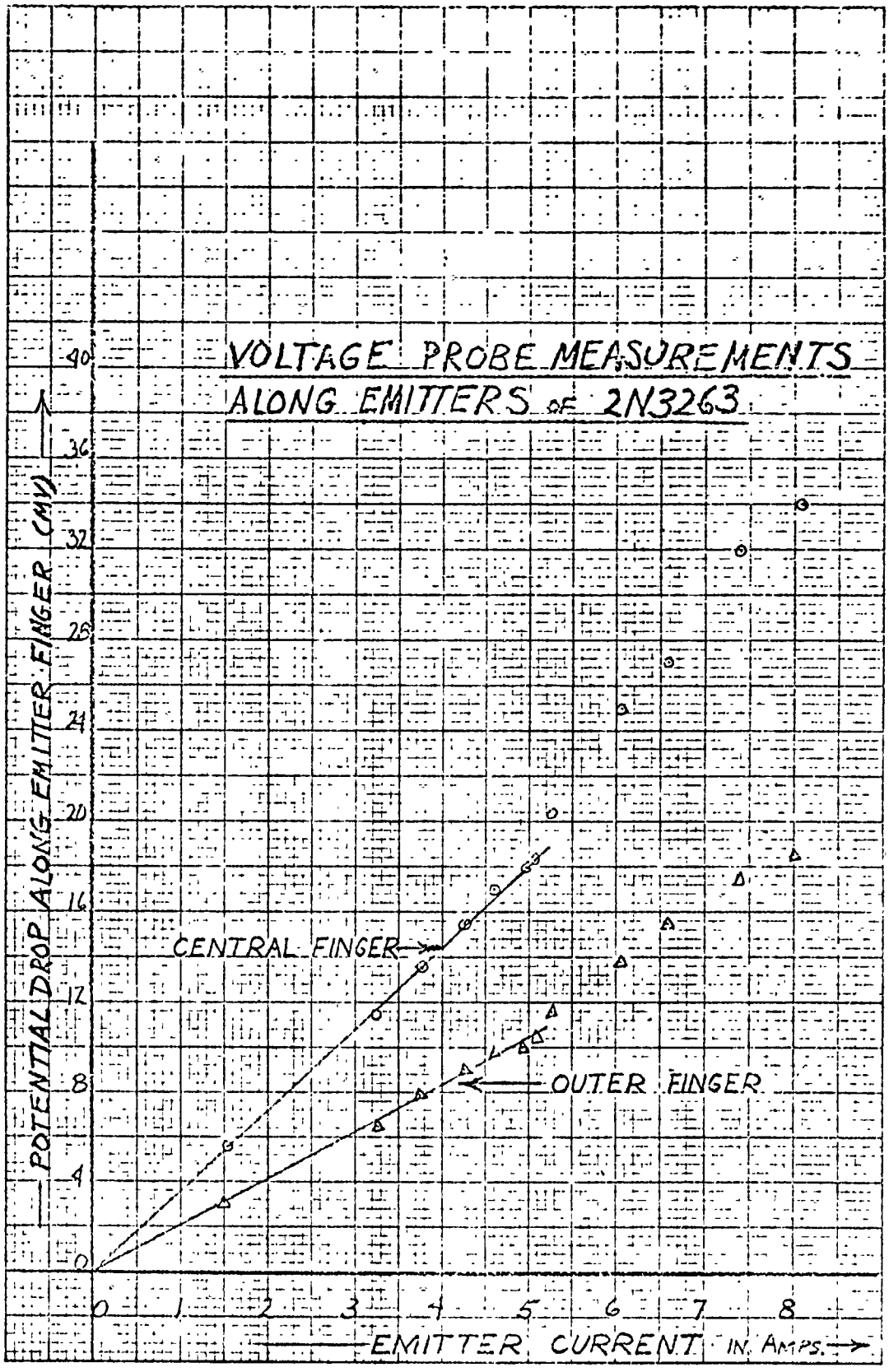


FIG. 15a

I_C(A)	I_B(mA)	Central Emitter Finger		End Emitter Finger		V_{CB} volts
		ΔV_{EB}	$\Delta V_{EB}'$	ΔV_{EB}	$\Delta V_{EB}'$	
1.5	20	725 mv	720 mv	725 mv	720 mv	+0.40
3.0	30	705	700	705	700	+3.0
5.0	50	730	720	735	725	+2.12
5.0	70	780	770	780	770	+0.52
7.5	70	705	685	715	695	+3.25

ΔV_{EB} refers to the base contact end; $\Delta V_{EB}'$ refers to the emitter contact end.

Table 2

B. Temperature Determination Using Liquid Crystals

Cholesteric liquid crystals were used very effectively to plot the isotherms on the surface of a 2N3263 transistor chip while operating in the active region [12]. Liquid crystals, useful in different temperature ranges, are readily available commercially[4] and their application on the surface of a silicon chip is easy and in no way effect the characteristics of the device. Some liquid crystals, when observed in white light, change color over the complete spectrum (red to violet) due to a temperature rise of 1°C, while others require a change of 50°C or more for this change to take place. A variety of other ranges can be obtained by mixing two liquid crystals.

At first the various liquid crystals to be used had to be calibrated for color versus temperature. For this purpose, thin aluminum lines were fabricated on small glass slides by the process of evaporation, photoresisting

4. For example Vari ight Corporation, 9770 Conklin Road, Cincinnati , Ohio.

and then etching. Standard microelectronic techniques were used and line widths from 10 to 40 mils were obtained. The geometry of the aluminum patterns used are shown in Fig. 16.

The effectiveness of using liquid crystals to detect temperature changes on the surface of the actual transistor chip was tested with the help of these slides by passing current through these Aluminum lines and observing the color changes. From the color patterns observed and some calibration curves, it was possible to plot the isotherms for these thin aluminum lines. The reason for using aluminum is obvious as the emitter and base metallization in an actual transistor is also aluminum.

For calibration purposes these slides were placed in a grooved recess on top of an accurately controlled hot-plate. A thermocouple was also connected beneath the slide. A drop of liquid crystal was placed on the slide (pre-blackened liquid crystal or, if the liquid crystal is colorless, then a base coat of some inert black paint is applied[5] to the surface before putting on the liquid crystal for better detection and contrast of colors). The temperature of the slide was raised very carefully and the various color changes of the liquid crystal were observed. Thus in this way the various available liquid crystals were accurately calibrated for color change versus temperature. A typical set of calibration data is shown for Vari-light Corporation's liquid crystals solution VL-126190 which is effective in the range 126 to 190°C, is shown in Table 3.

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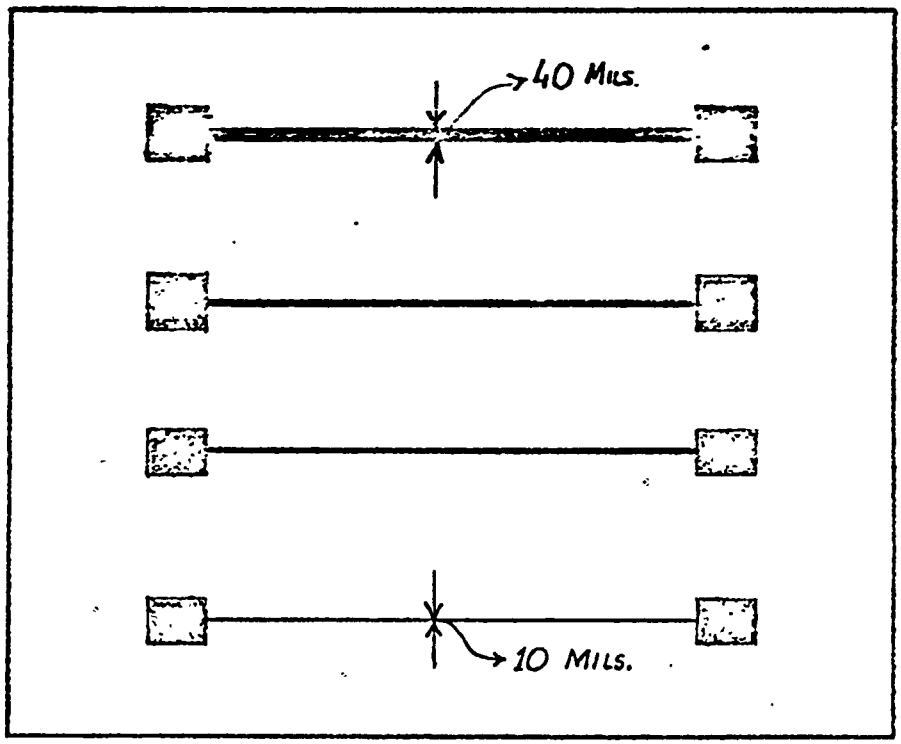
5. This black paint can later be removed easily using petroleum ether.



LINE PATTERN FOR TEMPERATURE CALIBERATION OF LIQUID CRYSTALS

FIG. 16

VL - 126190

LIQUID CRYSTAL SOLUTION

Color	Temperature
Colorless	> 190°C
Colorless to Violet	190°C
Violet Center	133°C
Violet to Blue	170.5°C
Blue Center	165°C
Blue to Dark Green	160°C
Dark Green Center	156.25°C
Dark Green to Light Green	148°C
Light Green Center	145°C
Light Green to Orange	140°C
Orange Center	138°C
Orange to Red	133°C
Red Center	130.5°C
Red to Colorless	126°C
Colorless	< 126°C

Table 3

Temperature isotherms on the surface of a 2N3263 transistor chip operating in the active region[6] were now plotted. A plot of these isotherms is shown in Fig. 17. While observing the temperature distribution on the nine emitter fingers of this interdigited device, the fingers were electrically probed, yielding the base-emitter voltage, V_{BE}, at various points along each of the emitter fingers. Assuming that this measured voltage was essentially across the emitter-base junction[7], the average emitter current density at each point was calculated using the expression

$$J_E = AT^3 \exp(-E_g/\eta kT)\exp(qV_{EB}/kT) \qquad (44)$$

The calculated average current densities at various points along the central emitter finger of this device are plotted in Fig. 18.

Since η in Eq. (44) lies between 1.0 and 2.0 but is unknown, three different curves are plotted for assumed values of η = 1.0, 1.5 and 2.0. In spite of the fact that this uncertainity in η doesn't permit calculation of the absolute value of the current densities, the relative current distribution indicated in Fig.18 is seen to be independent of η. This graph shows a peaking of current density about half-way along the central emitter finger and a tendency toward current cutoff at the end of finger furthest from the emitter feed lead.

Another set of curves depicting the current density variation along each of the nine emitter fingers is shown in Fig. 19. Here an average value of η = 1.5 is assumed for calculation purposes. In almost all cases the

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6. The device was operated at an emitter current of 3 Amps and a collector potential of 3.7 Volts.
7. The $I_B R_B$ base resistance drop was assumed to be negligible.

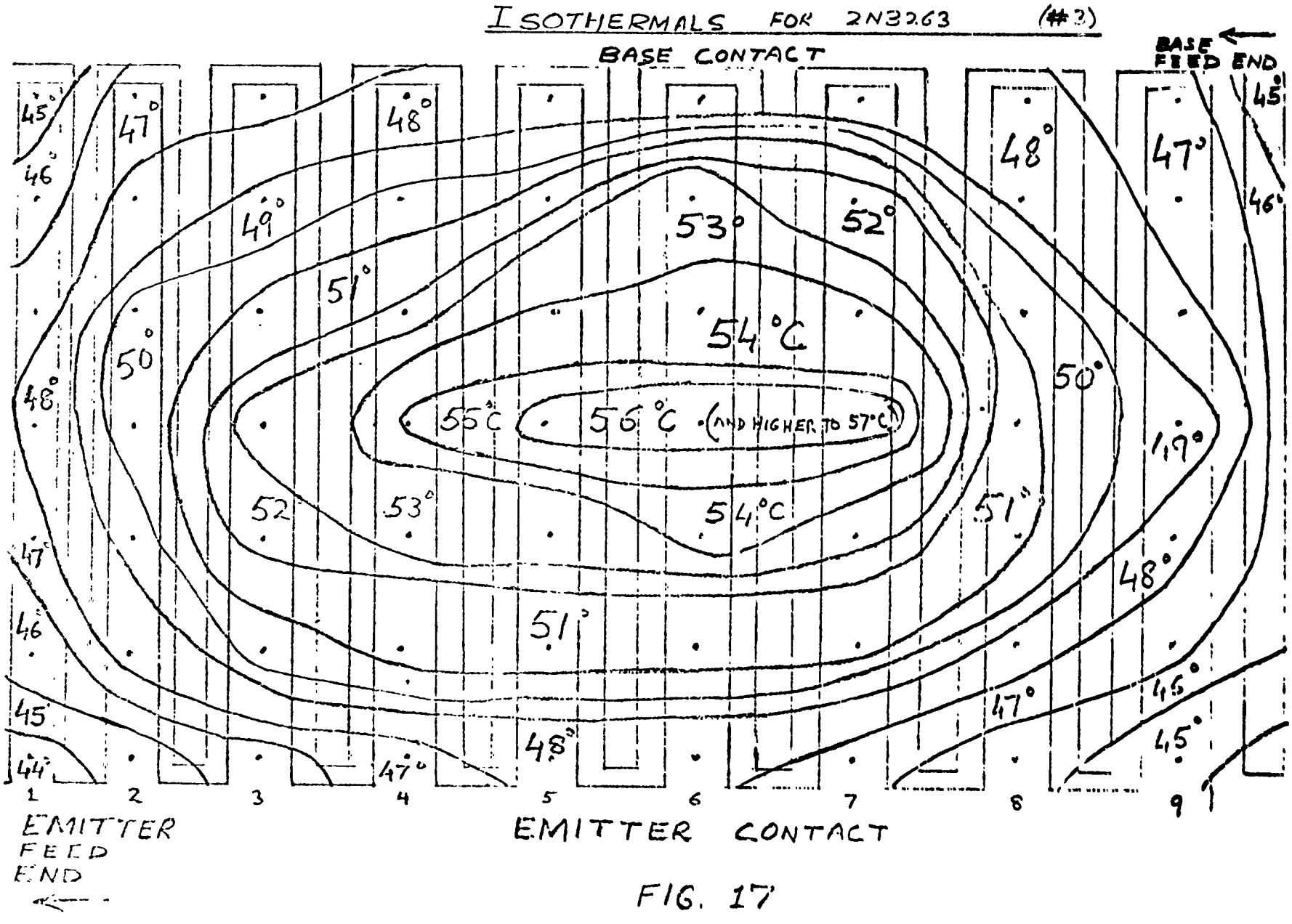

ISOTHERMALS FOR 2N3263 (#3)
BASE CONTACT
BASE FEED END
45°
47°
48°
48°
47°
45°
46°
49°
53°
52°
46°
51°
54°C
50°
50°
48°
55°C
56°C (AND HIGHER TO 57°C)
49°
52
53°
54°C
51°
47°
48°
46
51°
45
47°
45°
44°
48°
45°
47°
1
2
3
4
5
6
7
8
9
EMITTER FEED END
EMITTER CONTACT

FIG. 17

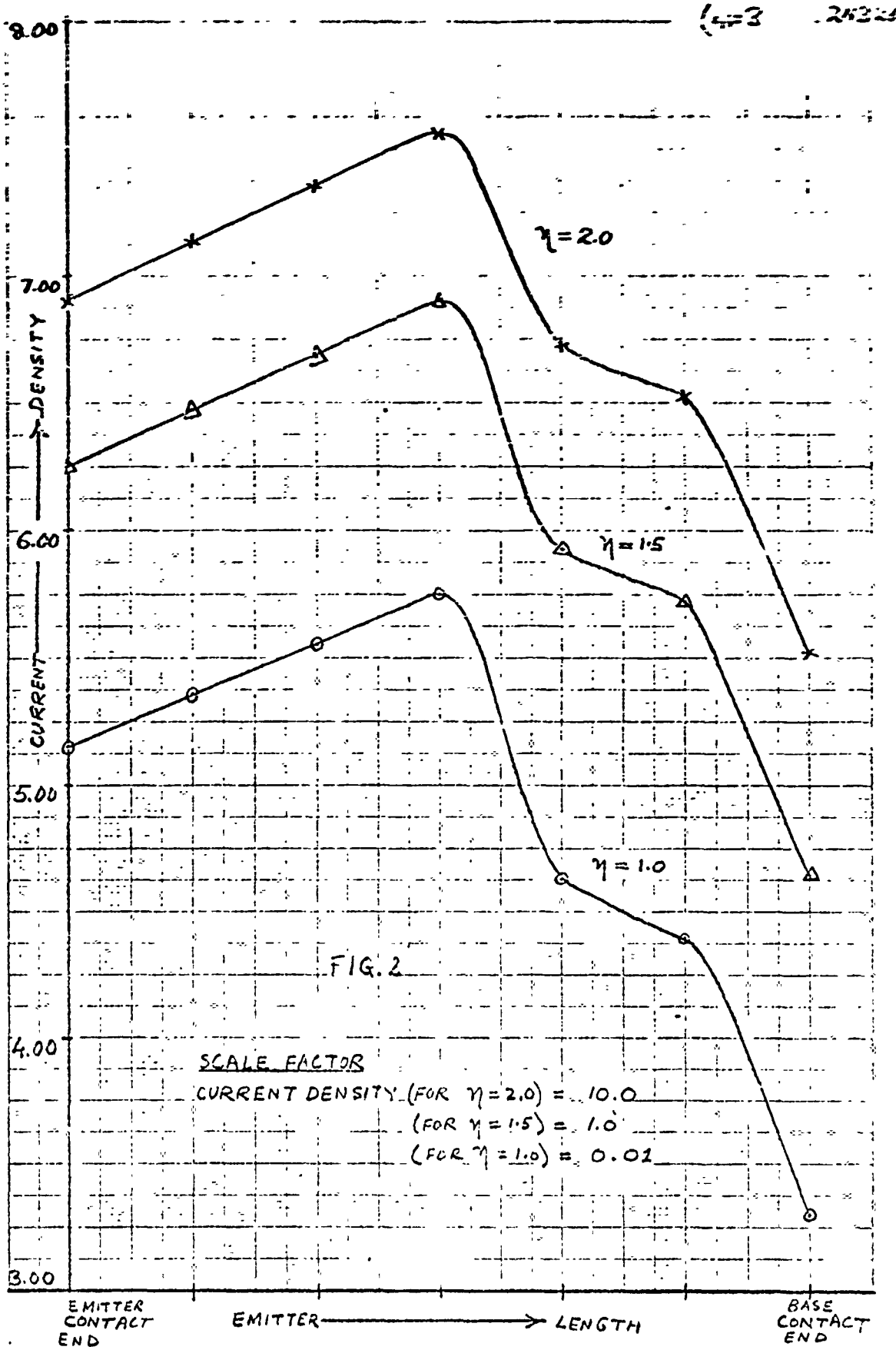

8.00
7.00
6.00
5.00
4.00
3.00
CURRENT DENSITY
η = 2.0
η = 1.5
η = 1.0
SCALE FACTOR
CURRENT DENSITY (FOR η = 2.0) = 10.0
(FOR η = 1.5) = 1.0
(FOR η = 1.0) = 0.01
EMITTER CONTACT END
EMITTER → LENGTH
BASE CONTACT END

FIG. 2

Fig. 18.

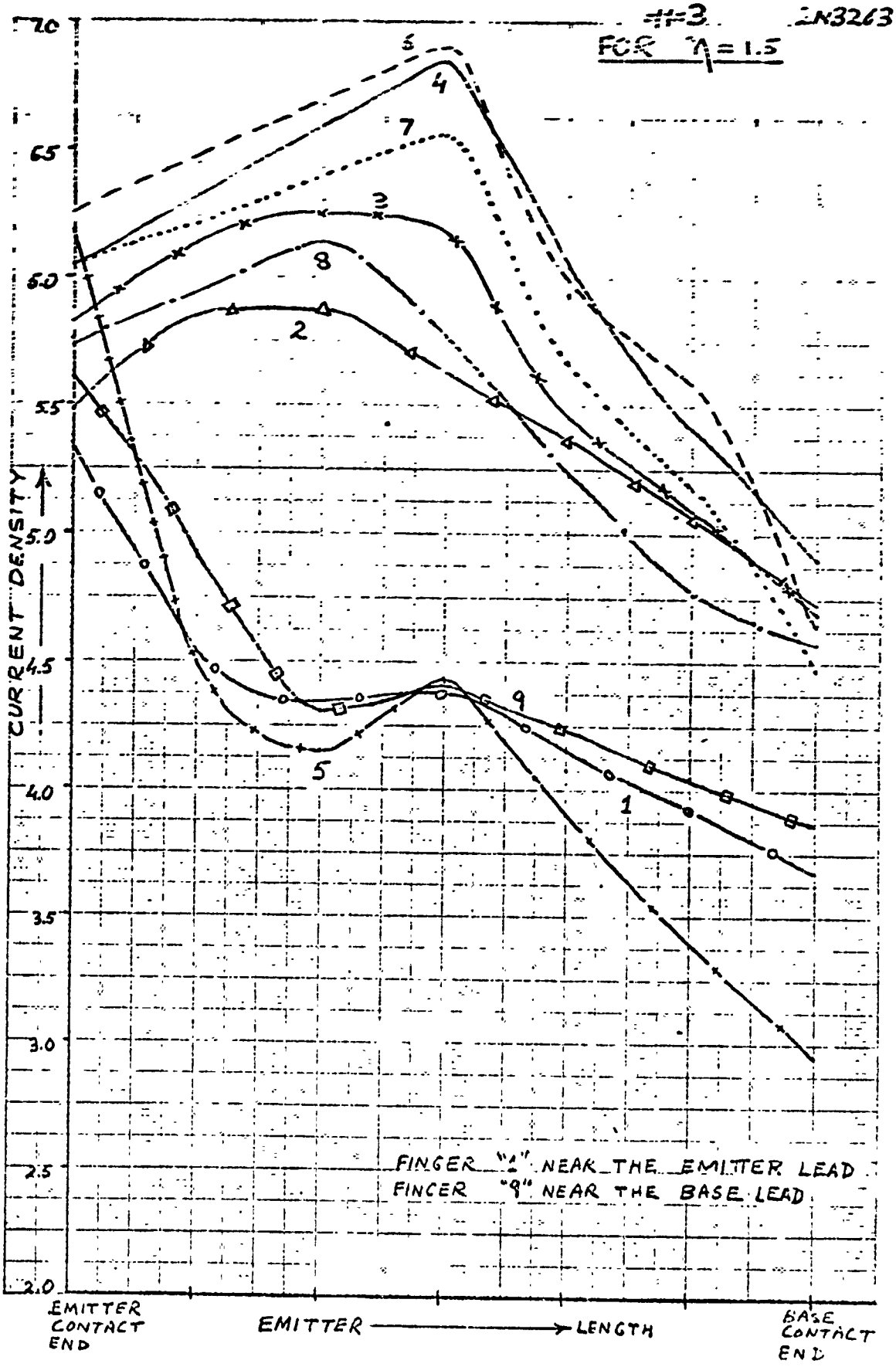

#3 2N3263
FOR A = 1.5
7.0
6.5
6.0
5.5
5.0
4.5
4.0
3.5
3.0
2.5
2.0
CURRENT DENSITY
FINGER "1" NEAR THE EMITTER LEAD
FINGER "9" NEAR THE BASE LEAD
EMITTER CONTACT END
EMITTER ——→ LENGTH
BASE CONTACT END

Fig. 19.

current density again peaks nearly half-way along the various emitter fingers. A curious result however is the average current density in the two outer fingers (Nos. 1 and 9) is distinctly lower than all the other fingers with the exception of no. 5. Cooling at the edges of the chip would explain the lower current density estimated in the outer fingers but doesn't explain the lower current density in finger No. 5. This cannot be explained in terms of cooling via the emitter and base feed leads either. It is concluded that although the general form of the isothermals shown in Fig. 17 correspond to cooling from the edges of the chip, the symmetry of the temperature distribution is skewed away from the emitter feed lead. This can perhaps be explained by hot spots in the middle of finger Nos. 6 and 7, and hence the higher current density in these emitters as seen in Fig. 19. The low current density in finger No. 5 may be due to high series resistance.

Figs. 20a, 20b and 20c show color photos of the transistor chip coated with liquid crystals at various emitter current levels. The photo in Fig. 20a is taken at a comparitively lower emitter current than Fig. 20b and 20c and one can see that the heating is quite non-uniform and skewed towards the right. This non-uniformity is more pronounced in the photos of Fig. 20b and 20c, which are at almost double the current level as compared to Fig. 20a. Here it depicts quite distinctly that the left half of the transistor is rather cold as compared to the right half and that even in the right half some regions are more hot than the others, the difference being as much as about 60°C (between violet and red). This non-uniformity in heating of the transistor chip especially at high current levels may be

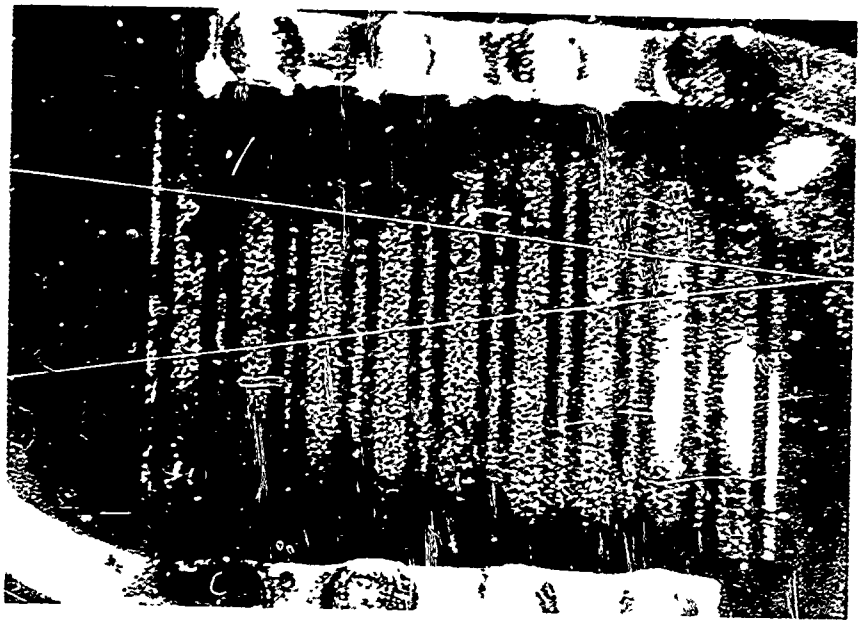


Figure 20a

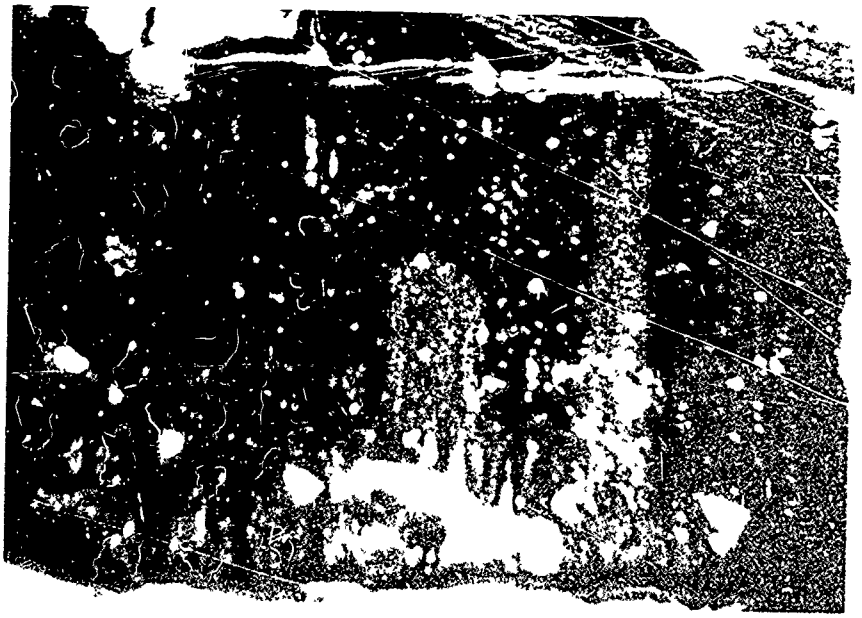


Figure 20b

Figure 20c

accounted for by improper heat sinking or the change of transistor characteristics and possible damage due to previous 2nd breakdown testing or other stressing. Dramatic skewing has been observed in transistors that have been previously tested numerous times for 2nd breakdown.

A similar isotherm plot was made, this time for a brand new transistor, untouched except by the manufacturer. This plot is shown in Fig. 21. From this again the transistor chip is hottest near the center, with the hottest portion again slightly skewed towards the right. The 9th finger (finger on the extreme right) is hotter as compared to finger 1 (extreme left). This may be why fingers 1 and 2 are carrying less current than the others as shown in Fig. 22 which depicts a plot of the calculated current density for the various fingers for $r_i = 1.5$. It appears from these curves that the bottom left hand corner of the transistor chip is the coldest and conducts minimum current as compared to the rest of the transistor chip. Fingers 5,6,7 being the hottest carry the maximum current.

The conclusion that can be drawn from all of these curves is that the central portion of the transistor chip in general conducts most of the current. The boundary of the chip conducts much less current, particularly the corner near the emitter lead end. Another point to note is that the emitter regions are hotter than the adjoining base contact areas since the former are carrying substantially more current. Hence, in fact, the area of the chip which is conducting is substantially less than the total chip area. This is in contrast to the case of a conventional thyrister in which nearly the whole chip conducts current when the device is switched on. This partially accounts for the vastly greater current handling capability of thyristers compared to transistors available commercially today.

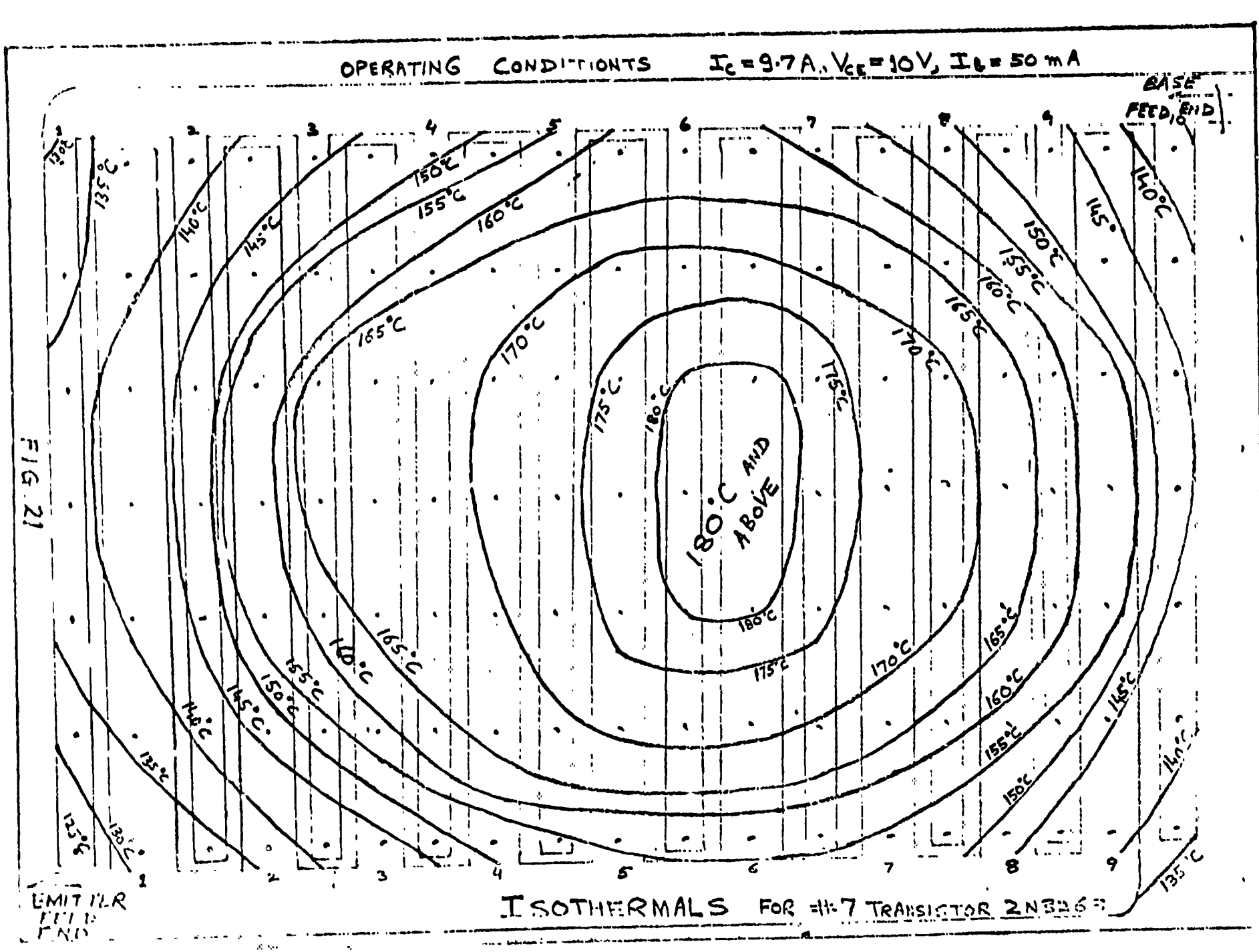

OPERATING CONDITIONTS $I_c = 9.7A., V_{CE} = 10V, I_b = 50\ mA$
BASE FEED END
130°C
135°C
140°C
145°C
150°C
155°C
160°C
165°C
170°C
175°C
180°C AND ABOVE
180°C
175°C
170°C
165°C
160°C
155°C
150°C
145°C
140°C
135°C
125°C
130°C
1
2
3
4
5
6
7
8
9
EMITTER FEED END
ISOTHERMALS FOR 11-7 TRANSISTOR 2N3263

FIG 21

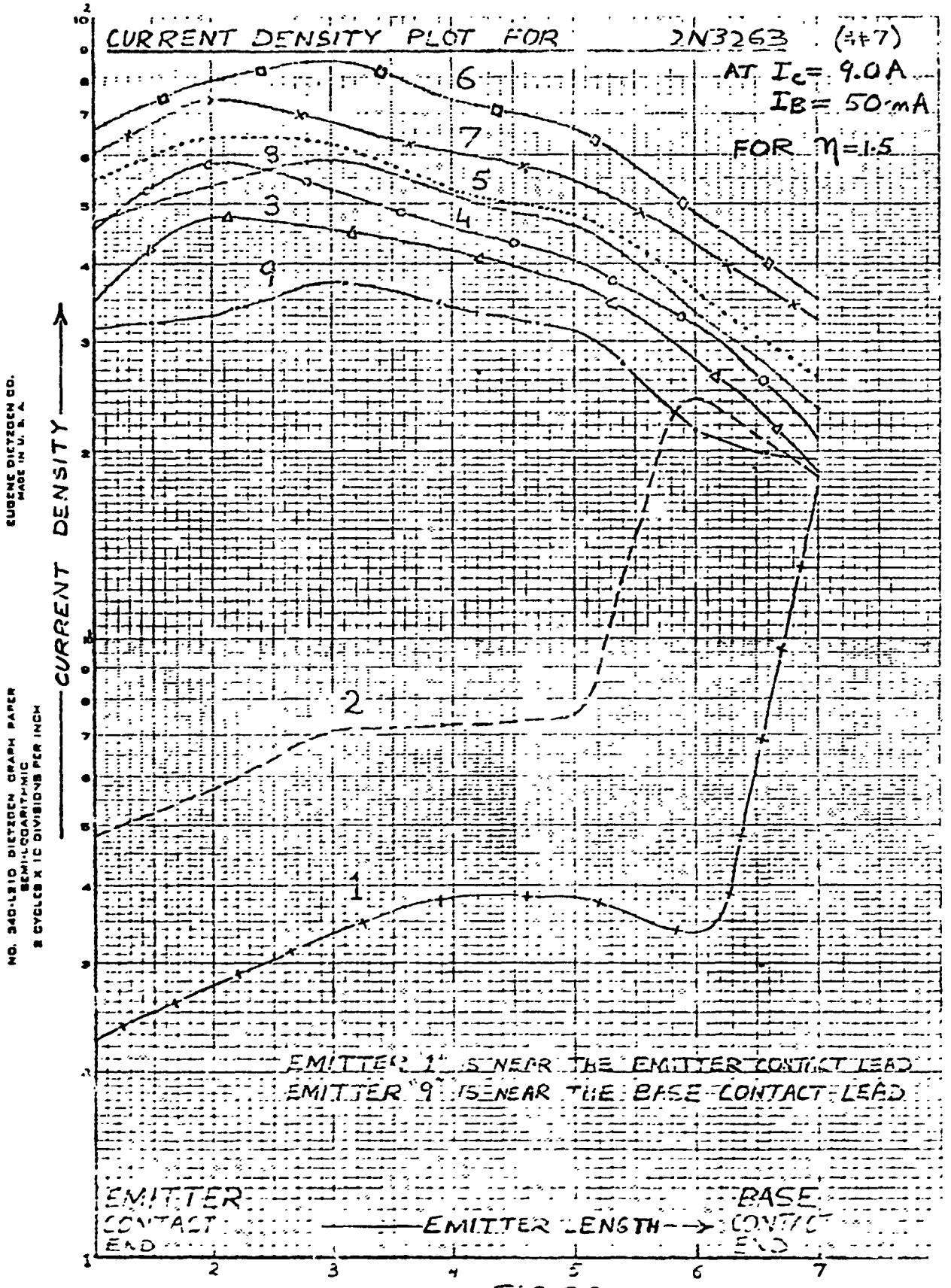

CURRENT DENSITY PLOT FOR 2N3263 (#7)
AT I_C = 9.0A
I_B = 50mA
FOR η = 1.5
6
7
8
5
3
4
9
2
1
EMITTER "1" IS NEAR THE EMITTER CONTACT LEAD
EMITTER "9" IS NEAR THE BASE CONTACT LEAD
EMITTER CONTACT END
EMITTER LENGTH →
BASE CONTACT END
CURRENT DENSITY →
EUGENE DIETZGEN CO. MADE IN U. S. A.
NO. 340-L210 DIETZGEN GRAPH PAPER SEMI-LOGARITHMIC 2 CYCLES X 10 DIVISIONS PER INCH

FIG. 22

B. Measurement of 2nd Breakdown Limitation on Commercial Power Transistors:

1. The Test Circuit:

In order to determine the second breakdown characteristics of various power transistors under DC and pulsed conditions, it is necessary to cause the device to go into a condition of second breakdown, detect this condition, and then immediately remove power from the device before it is destroyed. Fig. 23 shows a block diagram of the test set which was constructed to prevent destruction of power devices during forward-bias second-breakdown testing. This test set takes advantage of the distinct changes that occur in collector current and voltage at the initiation of second breakdown. The collector-emitter voltage of the transistor suddenly drops to a low value, while the collector current rises rapidly to a high value. This rapid rise of collector current is detected by the second breakdown (S/B) sensor, a low-inductance air-core transformer in series with the collector of the test transistor and coupled to a high gain amplifier. The output of the S/B sensor triggers the cut-out latch which reverse biases the series-pass transistor causing the collector current of the test transistor to decrease to zero.

The operating point at which the transistor is to be tested is established by adjusting the base drive to the test transistor and the power supply voltage, V_{CC}, which appears across the test transistor, series pass transistor, and a one ohm current sensing resistor. Once the desired level of collector current has been set by the Test Current Adjust potentiometer, it is maintained at that value throughout the test by a feedback network consisting of a current sensing resistor and differential

amplifier.

The collector-to-emitter voltage of the series-pass transistor is maintained at a constant value independent of test current by a feedback network consisting of a collector voltage sensor and a differential amplifier. This circuit is incorporated to insure that the series-pass transistor is operating in the active region during normal operation, thereby minimizing turn-off time of the test transistor when second breakdown occurs.

If the test transistor has large leakage current, or if a slow thermal runaway occurs, the collector current does not rise fast enough to be detected by the S/B sensor and other means must be used to protect the device. This is done by sensing the collector current level and triggering the cut out latch when this level exceeds a predetermined value.

The schematic diagram for the forward bias second-breakdown test set are shown in Figs. 24,25 and 26. This facility is capable of making second-breakdown tests at collector current levels up to 8 Amps and collector-to-emitter voltage levels up to 350 volts.

A test is initiated by either closing the Test switch for DC operation or applying a -10 volt pulse to the input of the current regulator for pulsed operation as shown in Fig. 24. The setting of the Test Current Adjust potentiometer determines the collector current level at which the test is being made. The current-sensing feedback loop is arranged so that only actual collector current flows through the one ohm sensing resistor, thus assuring accuracy of the test.

Stabilization of the current regulator is achieved by means of the 100 microfarad capacitor at the output of Q14 and the 0.039 microfarad

S/B TEST SET

BLOCK DIAGRAM

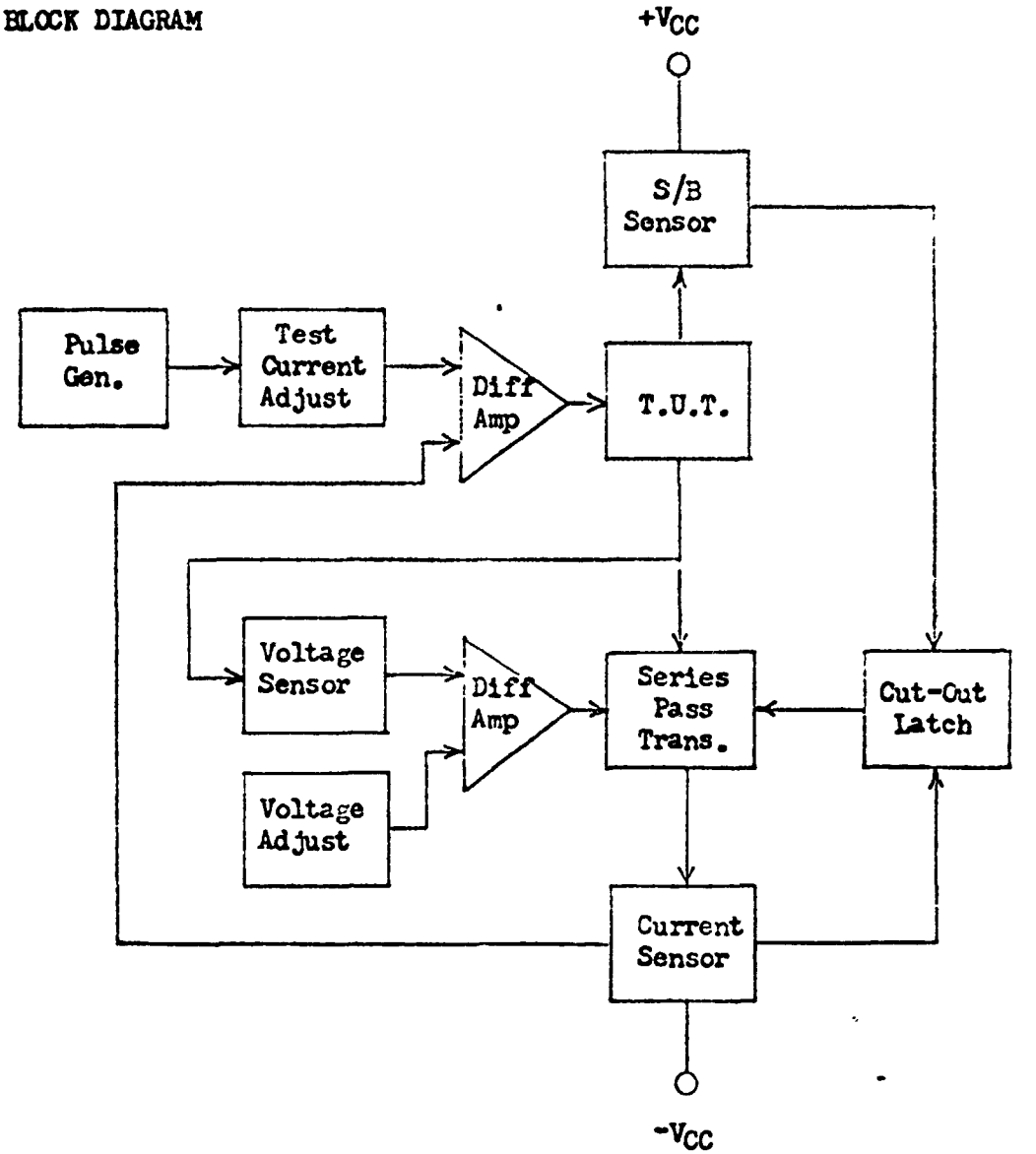
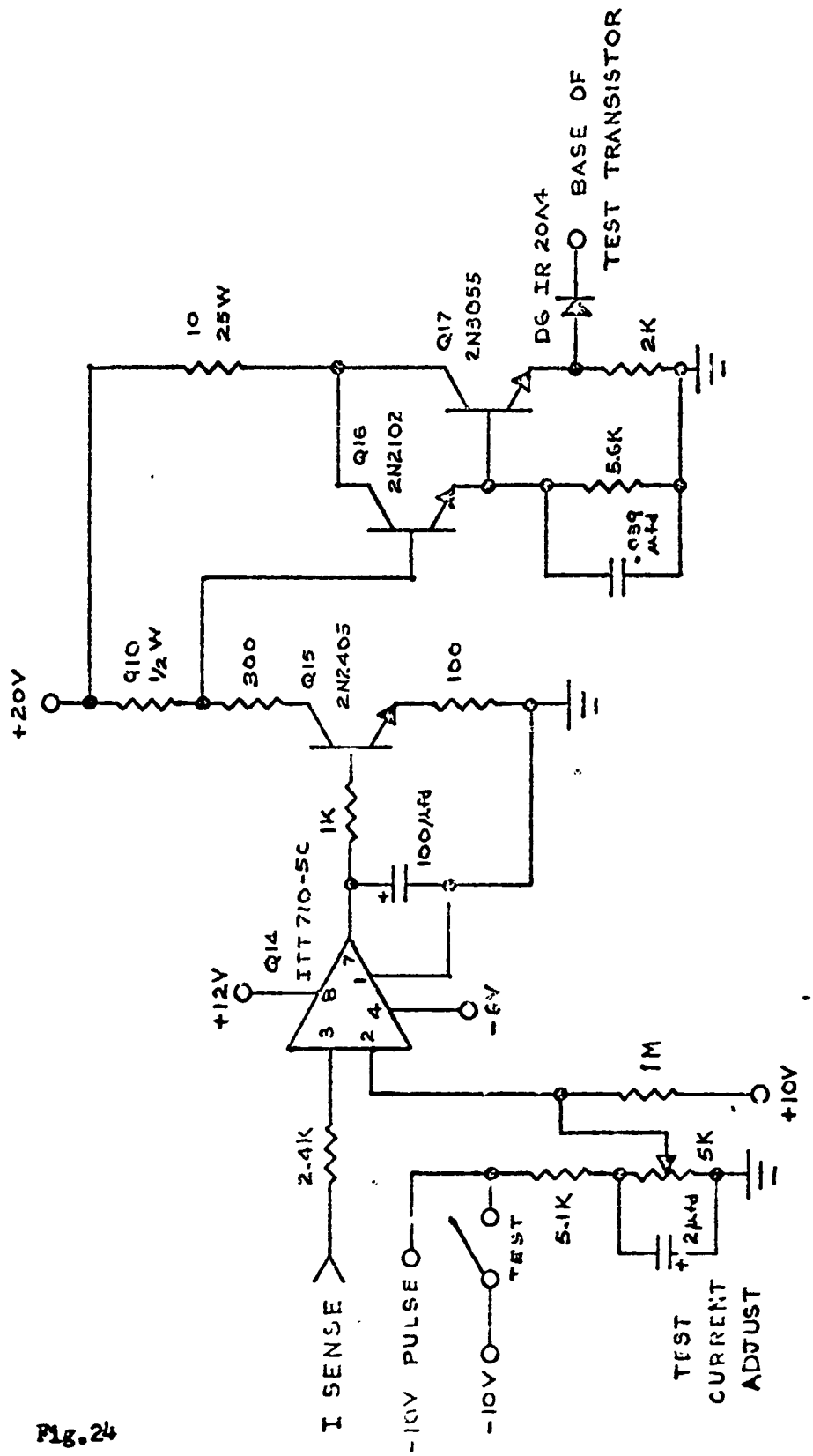


Fig.23

S/B TEST SET

Current Regulator



RESISTORS ARE 1/4 W UNLESS SPECIFIED OTHERWISE

Fig.24

capacitor at the base of Q17. It is difficult to stabilize the current regulator for all devices to be tested and at all test currents and voltages within the test set ratings because the gain-bandwidth product, f_T, of the test transistor depends on the particular device being tested and is a function of the voltage and current levels of the test. Also, the response time of the current regulator must be sufficiently slow to prevent the S/B sensor from triggering the cut-out latch at the beginning of a test which would incorrectly indicate a second breakdown. Because of these restrictions on the response time of the current regulator, the minimum test current pulse width that can be applied to the test transistor during pulsed operation is 10.0 milliseconds.

The circuit for regulating the collector-to-emitter voltage of the series-pass transistor is shown in Fig. 25. This voltage is varied by adjusting the voltage adjust potentiometer which establishes a reference voltage at the input of the differential amplifier, Q6. Stabilization of the voltage regulator is achieved by means of the 500 microfarad capacitor at the output of Q6 and the 0.015 microfarad capacitor at the base of Q9. Q18 and its associated circuitry maintain a charge on the 500 microfarad capacitor while the test set is in a latched condition. This speeds up the recovery time of the voltage regulator when the cut-out latch is reset. Q7 turns Q9 off during a latched condition which minimizes the current handling requirements of Q10, a low-power high-speed switch. This, and the operation of the series-pass transistors, Q12 and Q13, in the active region assure that the test transistor is turned off within one microsecond after second breakdown occurs.

Voltage Regulator

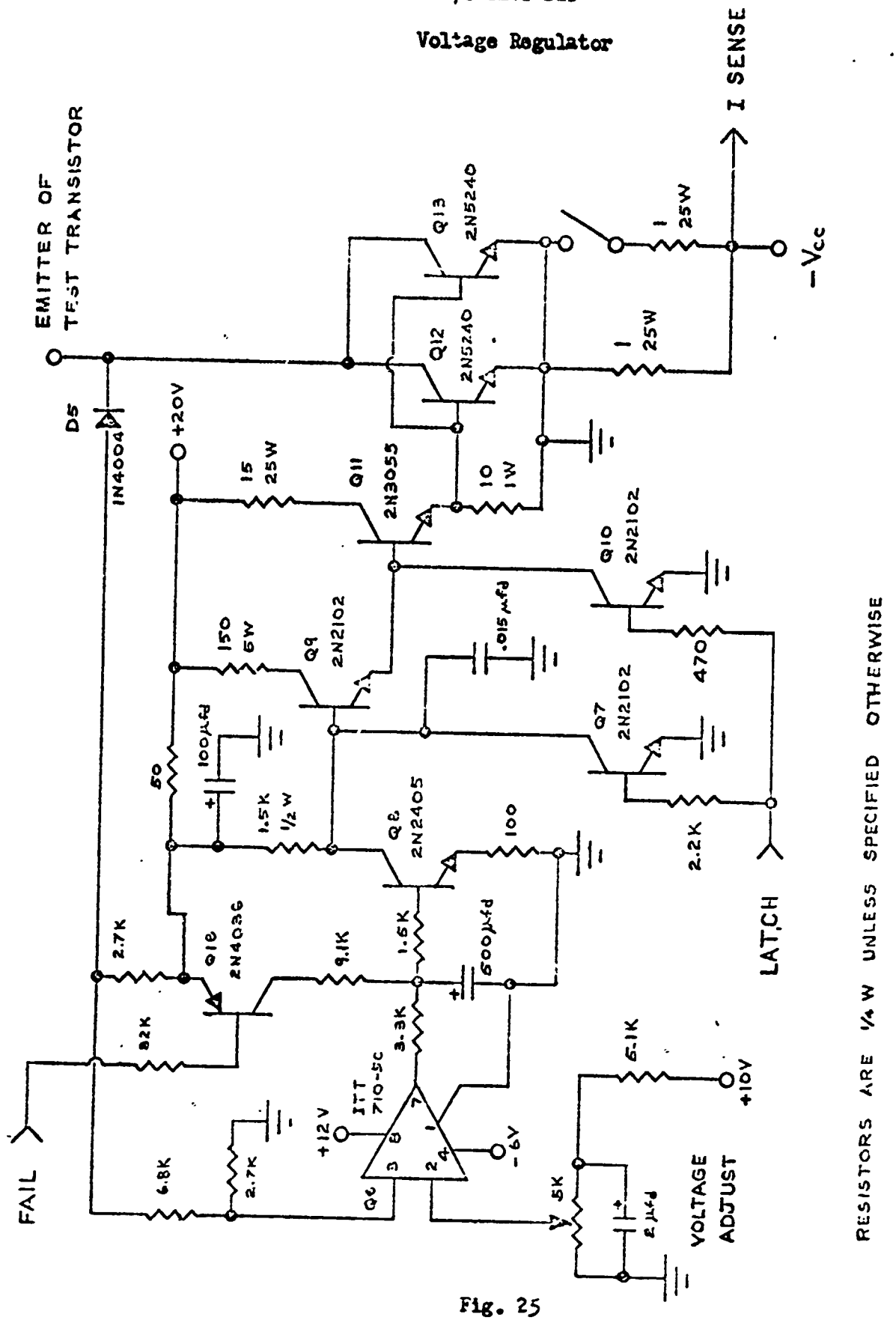


Fig. 25

When the second breakdown occurs, the rate of change of collector current is large, inducing a positive voltage at the input of differential amplifier Q2 as shown in Fig. 26. Overvoltage protection for the input of Q2 is provided for by diode D1 and the five kilohm potentiometer at the input of Q2 adjusts the sensitivity of the S/B sense circuitry.

Differential amplifier Q1 detects a condition of slow thermal runaway. The current level at which Q1 triggers is determined by the setting of the five kilohm potentiometer at the input of this amplifier. Diode D4 provides positive feedback for differential amplifier Q3. Thus, once a condition of second breakdown or slow thermal runaway occurs, Q3 will remain in a latched state until the reset push button is depressed, holding the test transistor in an off condition.

2. Experimental Results on Second Breakdown:

Experimental studies of the forward-biased second breakdown characteristics of various commercial power transistor were conducted under DC and pulsed conditions and for various device case temperatures. The S/B Test Set was used during these studies to prevent destruction of the devices being examined. To stabilize the case temperature of the device under test, all measurements were performed with the device mounted on a water cooled heat sink having a thermal resistance of approximately 0.1 degrees centigrade per watt. Device case temperature was monitored by means of a thermocouple affixed to the heat sink adjacent to the device.

The second breakdown locus for a given device is determined by first setting up the desired collector current level at which the test is to be made by means of the Test Current Adjust potentiometer. This is done with

S/B TEST SET

S/B Sense & Latch

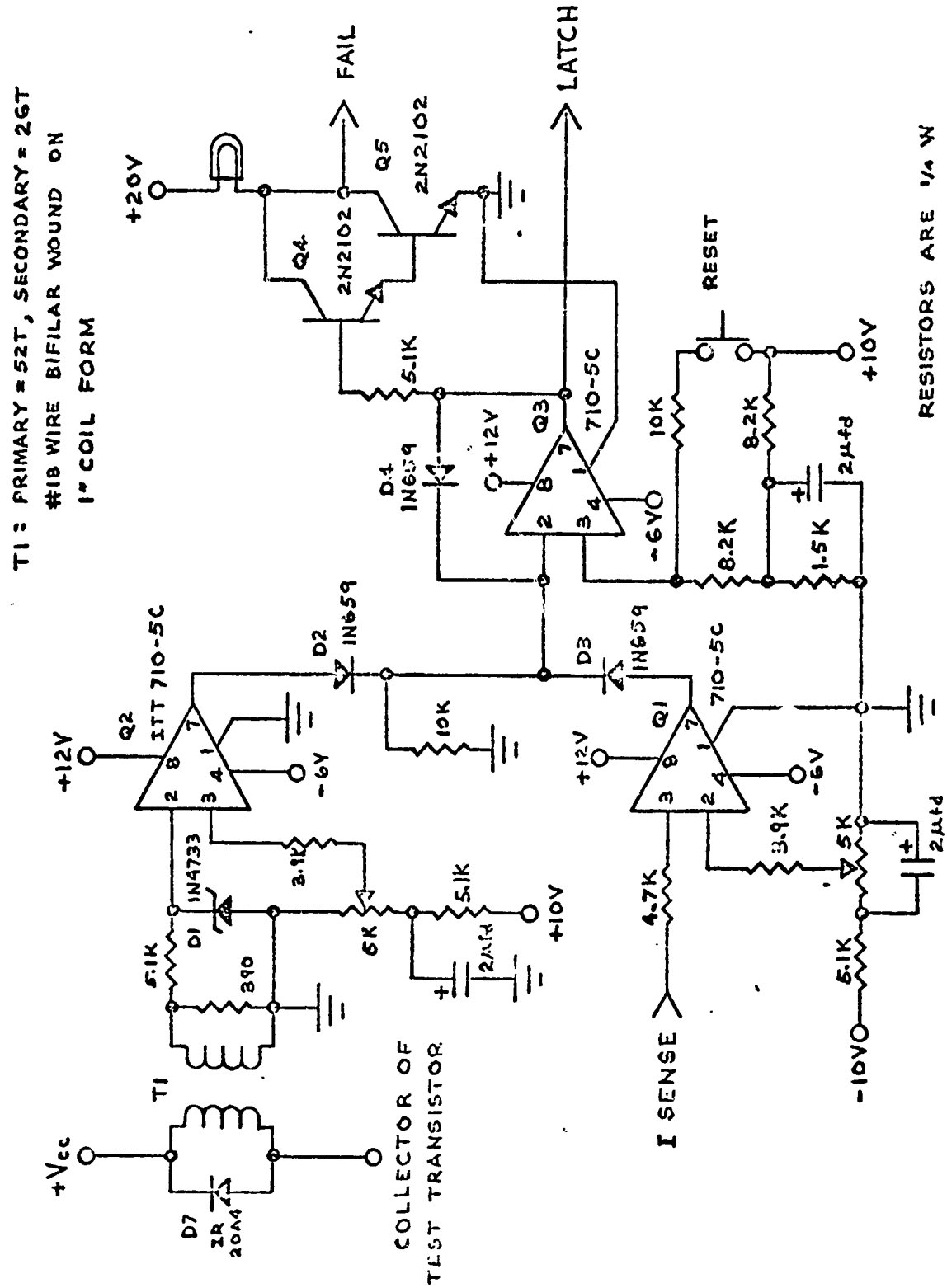


Fig. 26

the collector voltage supply set at some low value. Then the collector voltage level is incrementally increased until second breakdown occurs within the test period. After a single point on the curve has been experimentally determined, the validity of the measurement and an approximate indication of device degradation is checked by repeating the test with the collector supply voltage reduced by one volt; second breakdown should not occur within the test period.

The experimentally determined loci of the breakdown characteristics for the type 2N3054, 2N3772, and 2N3055 power transistors are shown in Figs. 27, 28 and 29, respectively. The type 2N3054 is a 4 ampere, 25 watt device; the 2N3772 is rated at 30 amps, 150 watts; and the 2N3055 is rated at 15 ampere and 117 watts. All are silicon devices having single diffused "homotaxial"structures. Base resistivity of these transistors is 7-12 ohm-centimeters and each has a base width of 0.65 mils yielding a minimum gain bandwidth product, f_T, of 800 kilohertz.

An estimate of the thermal-equilibrium junction temperature by means of the manufacturers specification of junction-to-case thermal resistance and experimentally determined second-breakdown power levels yielded expected junction operating temperatures in excess of 400 degrees centigrade if the devices were tested under DC conditions. Therefore, the S/B test time was limited to 2.5 seconds to prevent device degradation or destruction by normal thermal runaway.

The primary breakdown (P/B) loci in these figures are plots of open-base collector-to-emitter breakdown voltage for the respective devices. The similarity of the S/B characteristics of these devices such as: the power

BREAKDOWN CHARACTERISTICS

FOR 2N3054

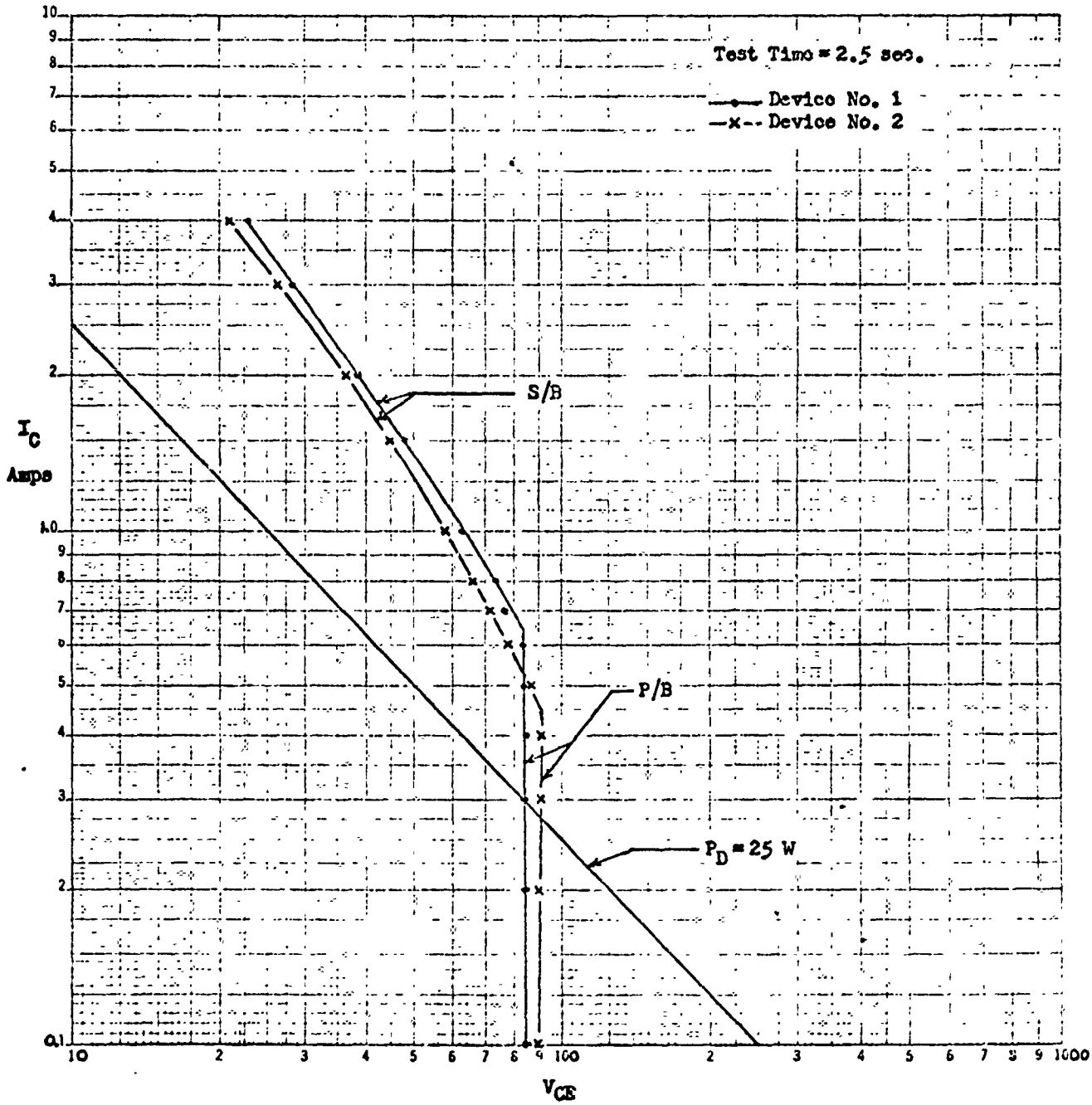


Fig. 27

Logarithmic 2 x 2 cycles

BREAKDOWN CHARACTERISTICS

FOR 2N3772

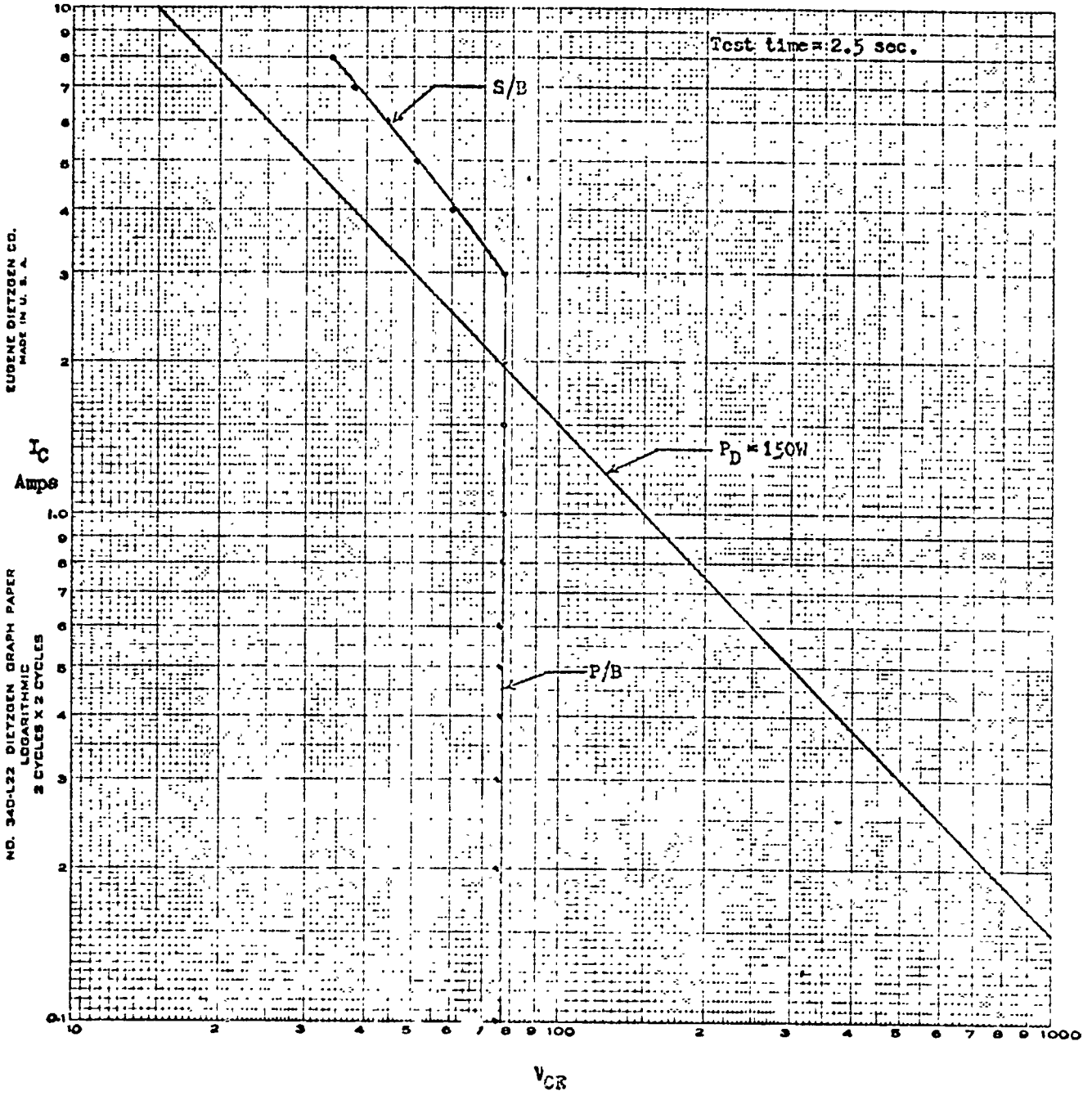


Fig.28

BREAKDOWN CHARACTERISTICS

FOR 2N3772

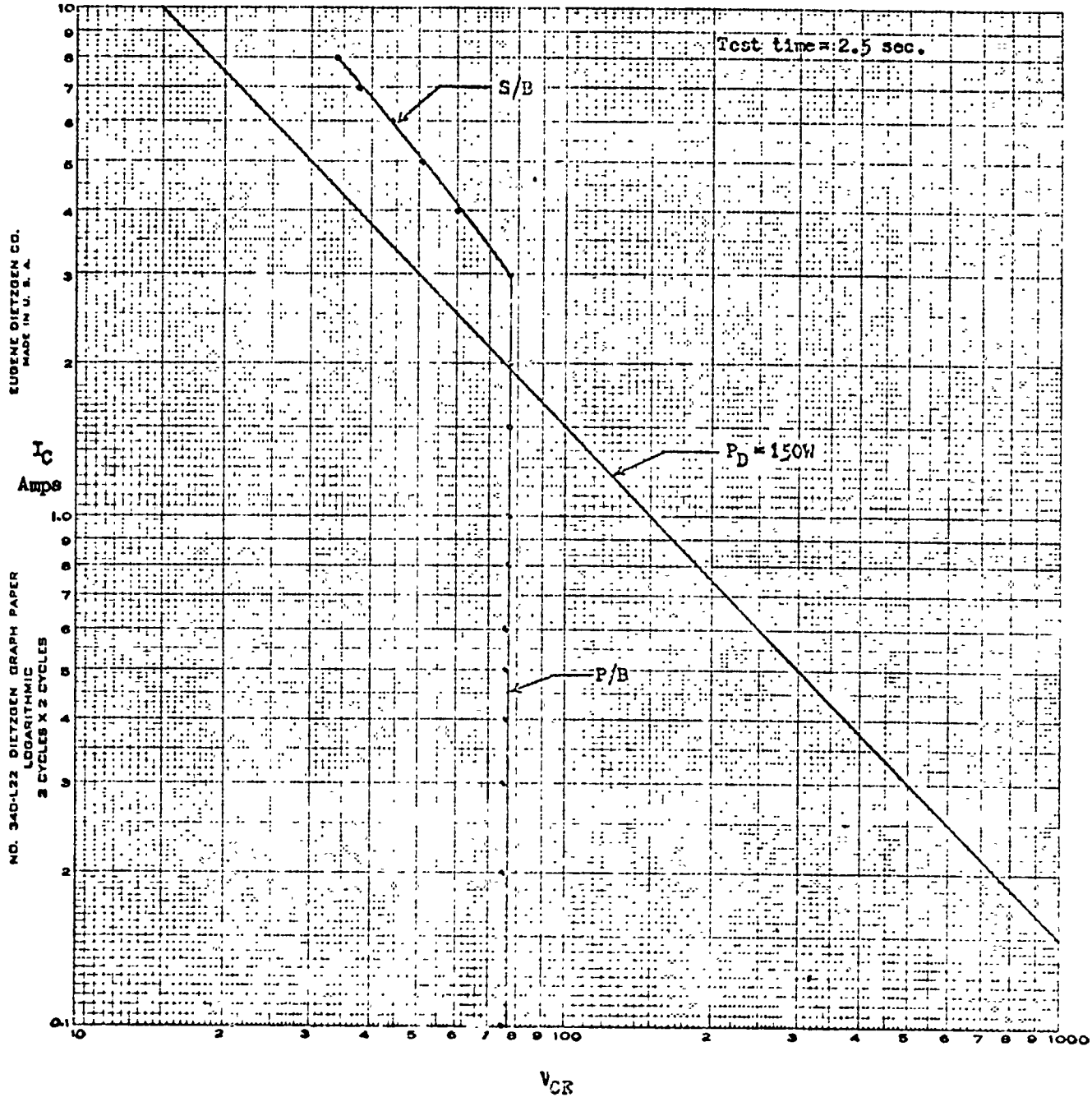


Fig.28

levels at which S/B occurs being much greater than the rated power dissipation levels and the concave downward shapes of the S/B loci may be attributed to the fact that the three types of devices tested have similar structures.

Results of a preliminary investigation of the temperature dependence of second breakdown are also shown in Fig. 29. In order to more accurately determine case temperature, these tests were conducted under DC conditions and S/B measurements were made only after the device had reached thermal equilibrium.

Breakdown characteristics for the type 2N3263 medium-frequency power device are shown in Figs. 30,31 and 32. This device is of the diffused emitter dual epitaxial layer type having maximum ratings of 25 amperes collector current and 125 watts collector dissipation. It has a base width of 0.10 mils and a minimum f_T of 20 megahertz.

Figure 30 clearly shows that for values of collector-to-emitter voltage greater than 25 volts and less than that which causes primary breakdown, the maximum DC power level the device can be operated at is determined by the DC S/B characteristics, not the maximum DC power dissipation rating of the device. Also, for a constant operating power level within this region, the device is more stable operating at low voltage, high current compared to operation at high voltage, low current.

A preliminary investigation of S/B characteristics as a function of collector current pulse width is shown in Fig. 31. Because of the previously mentioned limitations of the S/B Test Set under pulsed operation, modification of the present S/B Test Set or the construction of another test facility that will generate collector current pulse widths in the microsecond region is in order. High frequency behavior of S/B also needs to be investigated.

BREAKDOWN CHARACTERISTICS

FOR 2N3263

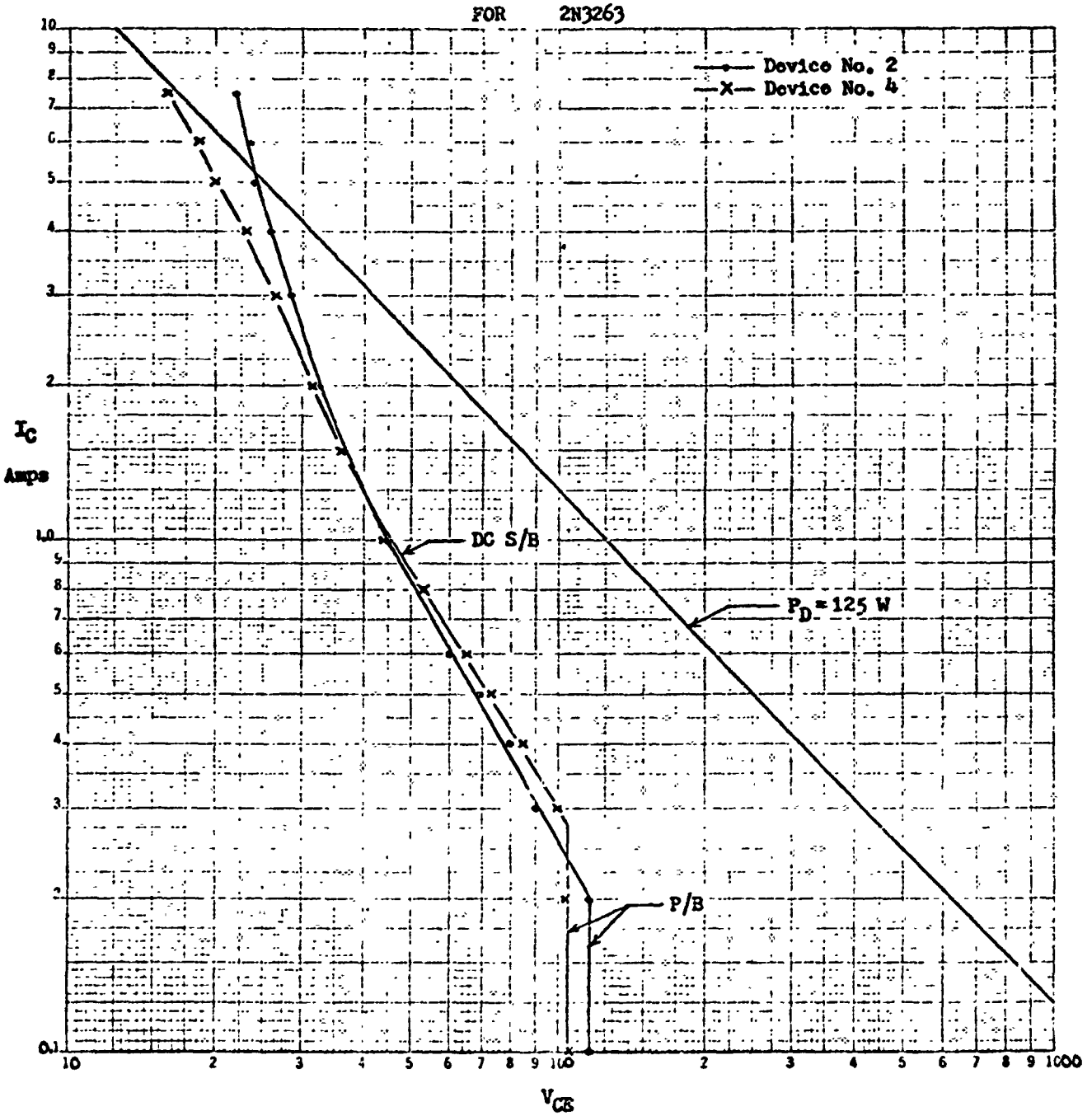


Fig. 30

Logarithmic, 2 x 2 Cycles

BREAKDOWN CHARACTERISTICS

FOR 2N3263

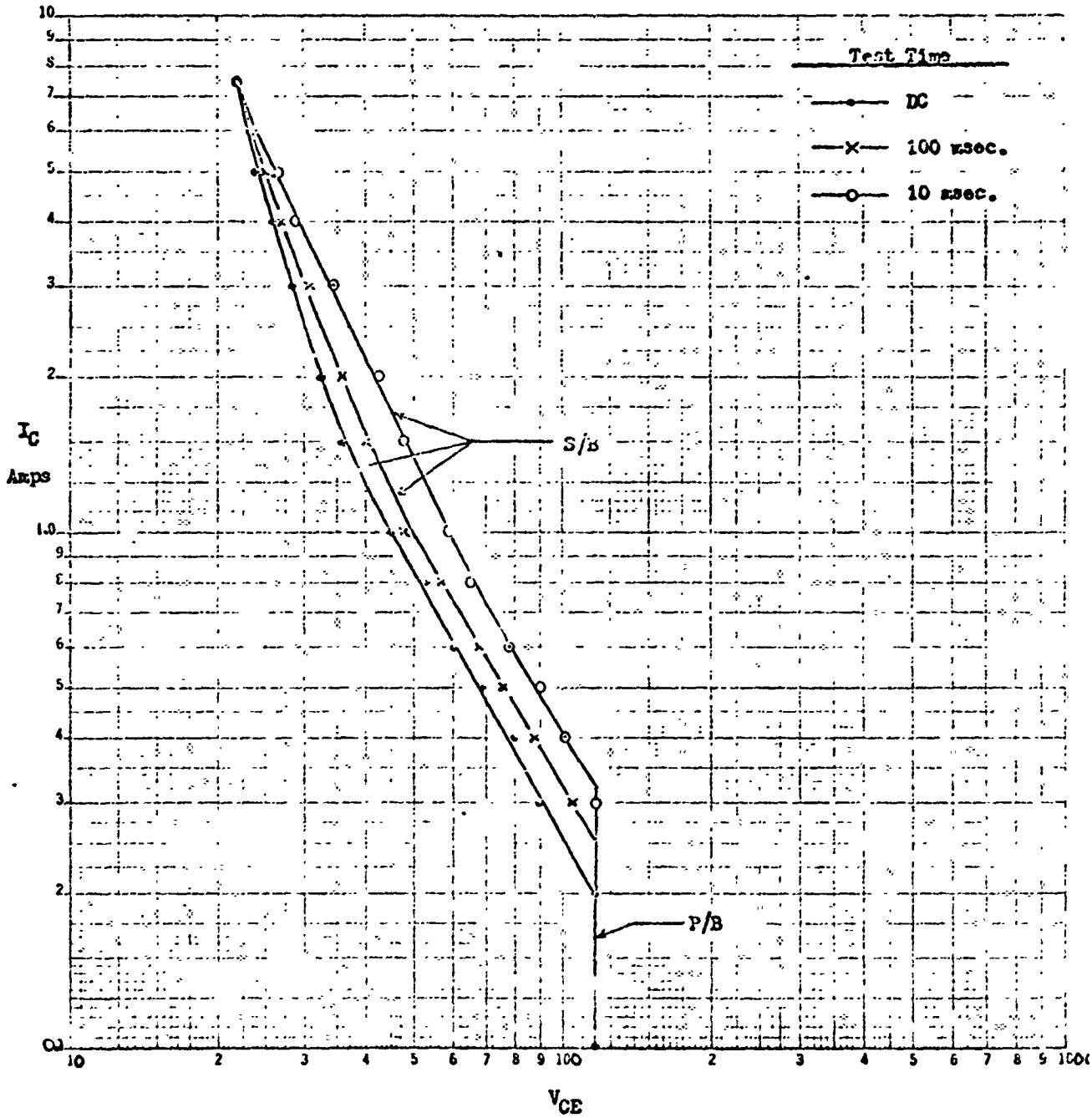


Fig. 31

Logarithmic, 2 x 2 Cycles

The temperature dependence of S/B for the type 2N3263 is shown in Fig. 32. It is interesting to note that for this device, an increase in case temperature while operating at *high current, low voltage* degrades device stability whereas it *improves* the stability of the device when operation is at *low current, high voltage*. This suggests further investigation of the temperature dependence of S/B with improved methods of controlling and measuring device temperature.

It was decided to investigate, in a precise manner, the concept of measuring the emitter-base diode voltage at a fixed value of current as an indication of device temperature. The question posed was, "where in the device structure is the temperature being measured by this technique?" Considering that the application of only 1 milliampere of current to a transistor such as the 2N2405 will provide uniform current flow and that this current is mainly provided by space-charge generated flow, the diode current-voltage relationship may be written as

$$I = BT^{3/2}\exp(-E_g/2kT)[\exp(qV/2kT) - 1]. \qquad (45)$$

The experimental verification of this relationship as a function of temperature is shown in Fig. 33 and yields a value for $B = 2.78 \times 10^{-3}$.

If this transistor is now operated at a high power level, the emitter current-voltage relationship may now be modeled as

$$I_E = A \sum_{i=1}^{n} \sum_{j=1}^{p} T^2\exp(-E_g/bkT_{ij})\exp(qV_{BE}/nkT_{ij}), \qquad (46)$$

where the two-dimensional transistor emitter is now considered to be composed of n x p individual emitters connected in parallel. This model

BREAKDOWN CHARACTERISTICS

VS. TEMP. FOR 2N3263

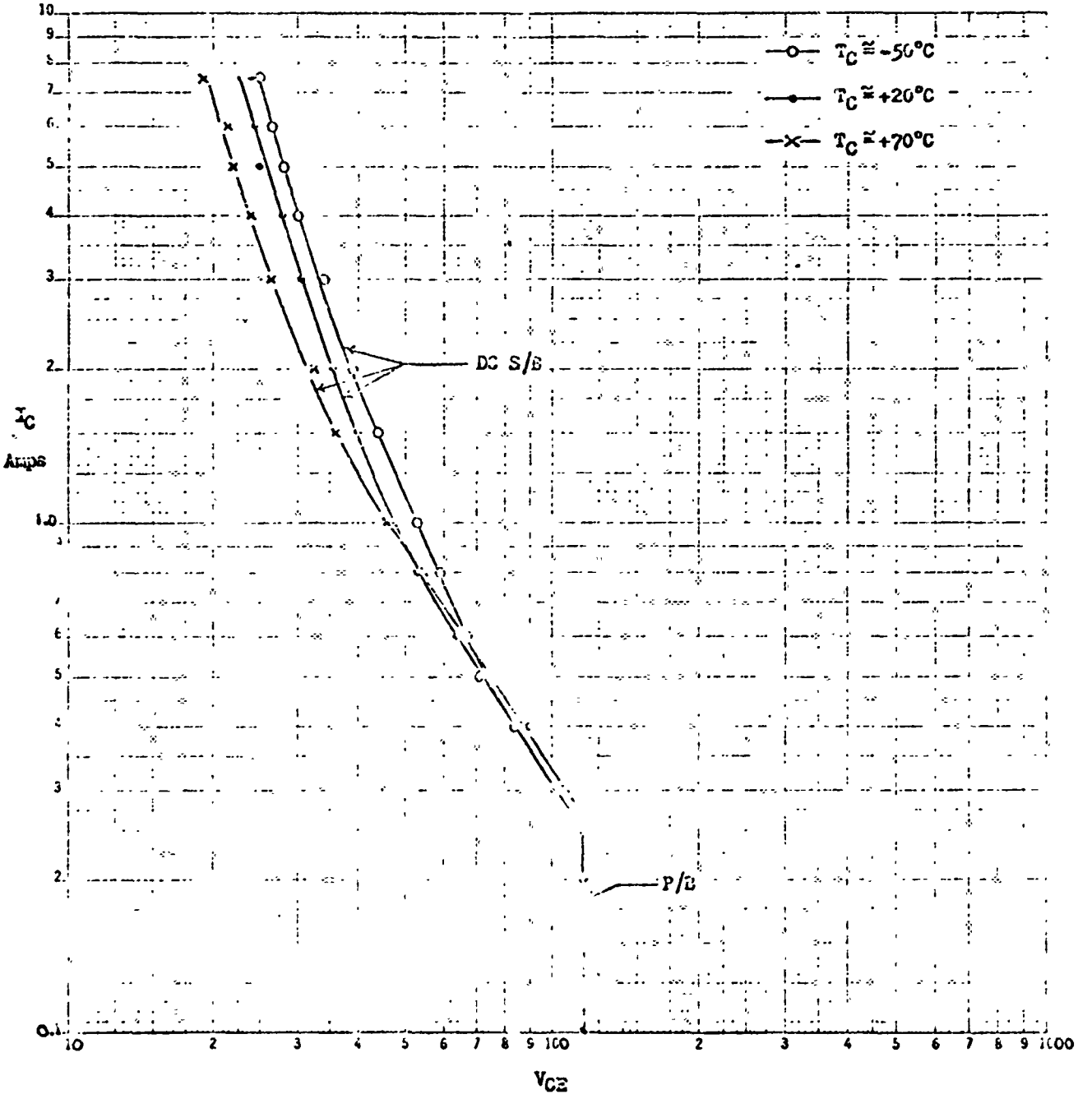


Fig. 32

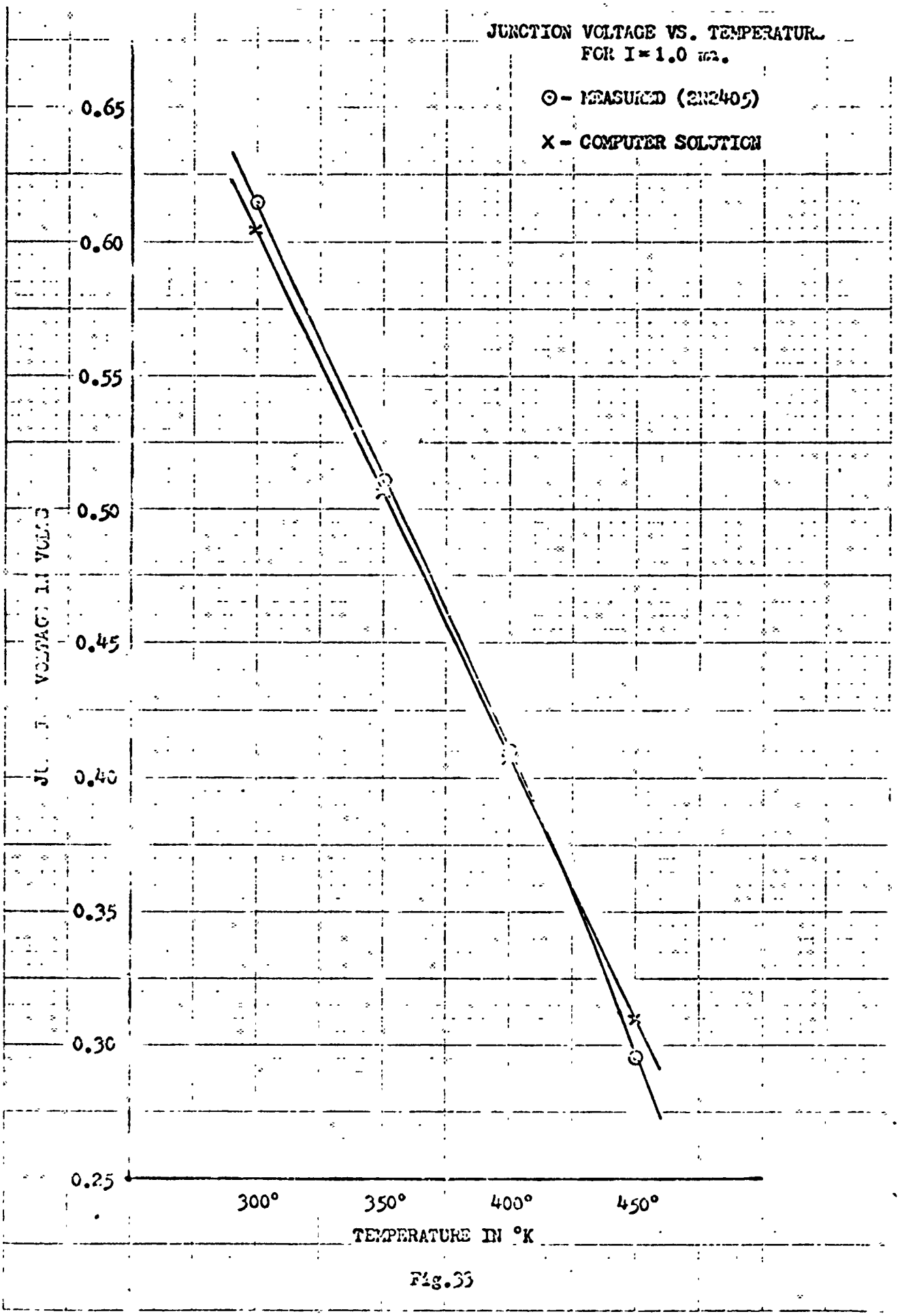

JUNCTION VOLTAGE VS. TEMPERATUR
FOR I = 1.0 ma.
⊙ - MEASURED (2N2405)
X - COMPUTER SOLUTION
0.65
0.60
0.55
0.50
0.45
0.40
0.35
0.30
0.25
300°
350°
400°
450°
TEMPERATURE IN °K

Fig.33

is the one that has previously been used in this program to calculate the current and temperature distribution in an emitter finger cross section, but their variations along the finger were ignored.

A computer program has been devised to yield a value for the emitter-base voltage for a transistor operating with an arbitrary temperature distribution, with a small current applied. This would tend to show what temperature is in fact being indicated by this technique of measuring the junction voltage for a small applied current.

It was found that for various temperature distributions such as a linear distribution, a gaussian distribution and a temperature impulse (corresponding to a "hot spot") yielded results that tended to indicate a junction temperature that was the arithmetic average of the assumed temperature distribution. The temperature which would be measured electrically by this technique for a typical emitter temperature distribution (previously calculated) is shown in Fig. 34. Again approximately an arithmetic average is "measured".

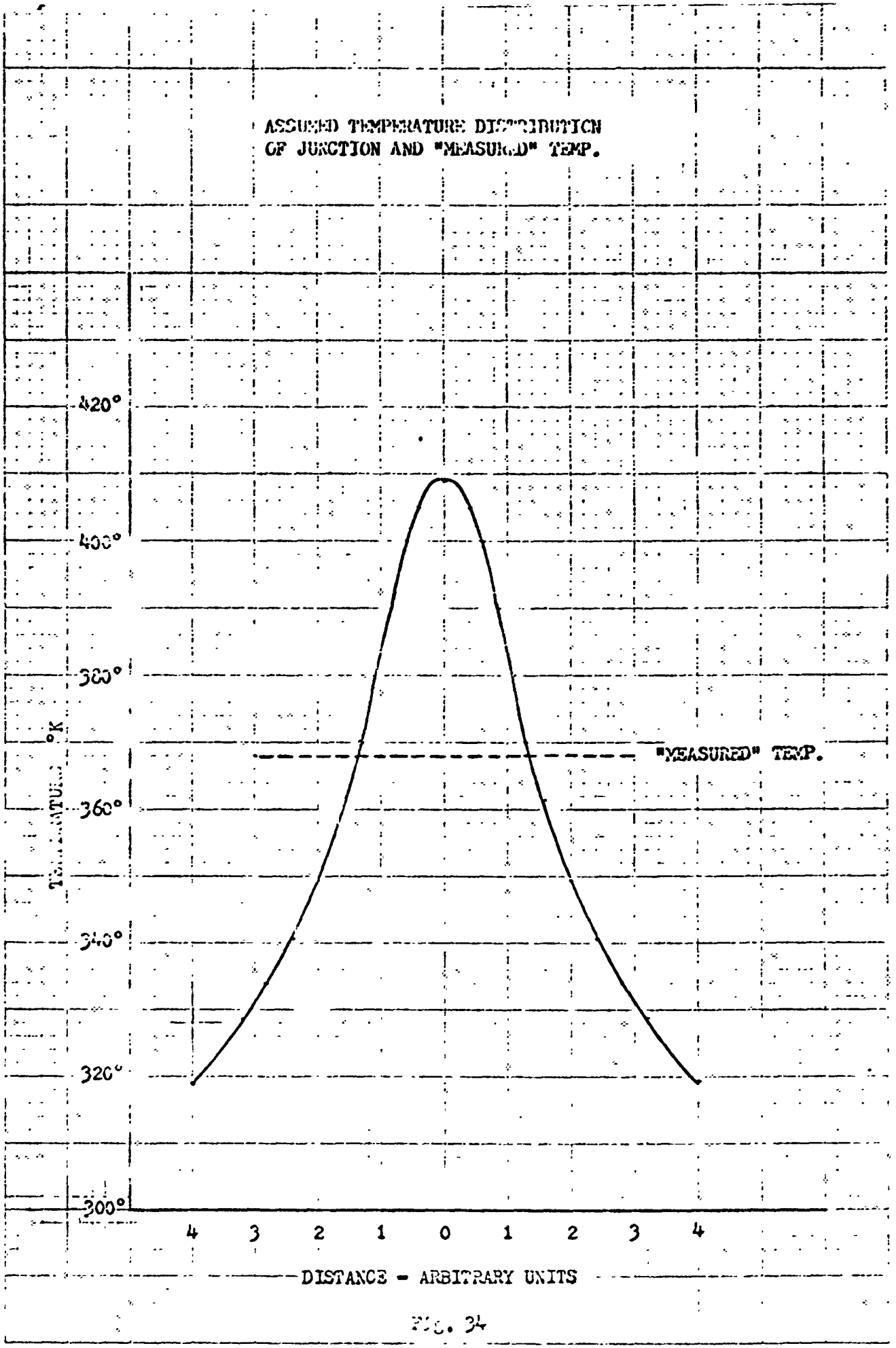

ASSUMED TEMPERATURE DISTRIBUTION
OF JUNCTION AND "MEASURED" TEMP.
420°
400°
380°
360°
340°
320°
300°
°K
"MEASURED" TEMP.
4 3 2 1 0 1 2 3 4
DISTANCE - ARBITRARY UNITS

Fig. 34

IV. METHODS OF IMPROVEMENT OF 2nd BREAKDOWN TRANSISTOR BEHAVIOR

The method of emitter ballasting to improve the second breakdown behavior of power transistors has been practiced for some time by manufacturers of these devices. Nichrome thin film resistors are usually deposited on the silicon chip and electrically connected in series with each of the emitter fingers of the interdigited device. Should a spurious hot spot occur in any one of these fingers, additional current will tend to be drawn by this emitter, causing an additional voltage drop across the ballast resistors in series with it, which in turn tends to reduce this current increase. This stabilizing feedback mechanism depends indirectly on the local temperature rise through a current increase which is sensed and limited by a ballast resistor. A more direct approach to the problem would be to sense the temperature rise directly and provide a feedback mechanism to cutoff the excess current flow caused by this temperature increase, since it is the latter which can destroy the device. A technique for accomplishing this end is proposed involving a thin film resistor with a negative temperature coefficient which shunts the emitter-base junction locally, thereby limiting the increase of current to an emitter finger which undergoes a spurious temperature rise. First the computation of the proper value of emitter ballast resistor for a given transistor design will be discussed.

A. Computer Calculation of the Stabilizing Effect of Emitter Ballasting:

The manner in which the maximum power that a given transistor design can handle (free from 2nd breakdown) can be calculated along the lines described in Section II. It is of interest to determine the improvement

in the power handling capability of a specified transistor design, caused by the addition of different values of ballasting resistors. The technique for carrying out this computer-aided calculation is as follows: First calculate the steady-state current density and temperature distribution in the emitter of a transistor of a given design operating at a certain power level, as indicated in Section II. Now note the emitter-base junction voltage, V_{BE}, which is needed to sustain the specified emitter current. Next assume a particular value of series ballast resistor to be placed in series with the emitter, calculate the voltage drop across the resistor due to the current flow and add this to V_{BE} to yield the applied voltage, V_A. Now assume a temperature impulse of a few degrees somewhere under the emitter and recalculate the current density distribution due to this incremental change in the temperature distribution. Then recalculate the new temperature distribution, etc., following the time-dependent heat flow analysis outlined in Section II, this time maintaining a fixed applied voltage, V_A. The emitter-base voltage, V_{BE}, at each instant is obtained by subtracting the drop across the ballast resistor from the assumed constant applied voltage, V_A. The criteria for 2nd breakdown is, as before, when each successive iteration yields continuously increasing temperature values. If stability is predicted by a settling down of the temperature rise due to the initial temperature impulse, successively higher applied voltages can be assumed until instability is predicted. Now the new power capability of the given transistor design with a specific value of ballast resistor has been determined. Calculations along these lines are being pursued and the stabilizing effect of emitter ballasting for different transistor designs are being investigated.

B. Temperature Sensing Stabilization:

In the Fourth Monthly Report a possible alternative to the idea of emitter ballasting was suggested. Since the temperature rise is the intrinsic cause of power transistor thermal run away, it was proposed that a temperature sensing device which automatically reduces the current flow to a locally heated emitter finger would be more appropriate than the current limiting action of an emitter ballast resistor. The scheme envisaged is shown in Fig. 35. The resistor marked R is a thin film semiconductor resistor which is in good thermal contact with the transistor and can bypass-to-ground excess base current caused by internal heating of the transistor. Since a germanium resistor has a negative temperature coefficient of resistance starting near 100°C, such a device would appear to be ideal for this purpose.

Hence it is of interest to compute the resistance variation of a pure germanium resistor in its intrinsic range. The germanium resistance value is given by

$$R_{Ge} = \frac{\ell}{\sigma A} = \frac{\ell}{n_i q(\mu_n + \mu_p)A}, \qquad (46)$$

where ℓ is the length and A the cross sectional area of the resistor, μ_n, μ_p are the electron and hole mobilities, n_i the intrinsic density of carriers and q is the electronic charge. Introducing the temperature dependence of n_i, μ_n and μ_p, Eq. (46) becomes

$$R_{Ge} = \frac{C}{T^{3/2} e^{-E_g/2kT} [\, 3900(300/T)^{1.7} + 1900(300/T)^{2.3} \,]} \qquad (47)$$

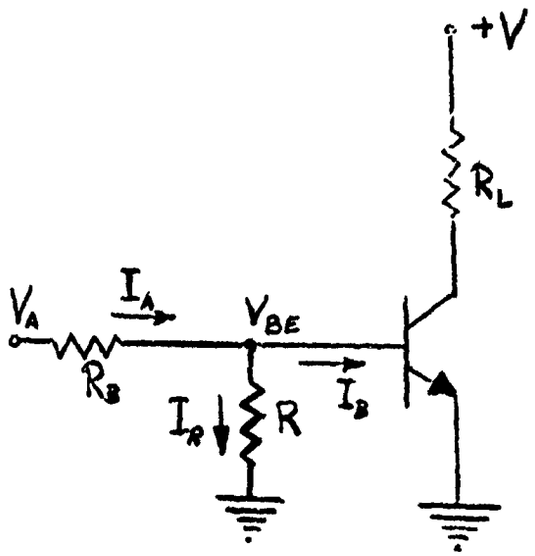


Fig. 35: Circuit for Transistor Thermal Stabilization Using a Semiconductor Temperature Sensing Stabilizing Resistor, R.

where C is a constant, independent of temperature. Since the exponential term dominates the temperature dependence, Eq. (47) may be approximated by

$$R_{Ge} \quad C' e^{E_g/2kT}. \tag{48}$$

Using instead the data on n_i for germanium of Morin and Maita

$$\frac{R_{Ge}@473°C}{R_{Ge}@373°C} \approx 22. \tag{49}$$

Hence the germanium resistance will decrease approximately by a factor of 22 as the transistor temperature rises from room temperature to 200°C.

If the transistor is driven from a current source, the decreasing value of the germanium resistor with transistor heating will tend to cause the input current to bypass to ground, preventing the device from overheating. If the transistor is driven from a voltage source, the germanium resistor will decrease in value below the resistor R_B in series with the transistor base connection and again the input current will be diverted to ground. The resistor R_B required will now be much lower in value than that needed to limit the base current, if no germanium shunting resistor were employed. An analysis indicates that the base resistor required is given by

$$R_B = \frac{\left[1 - \frac{1+\beta}{\gamma(\alpha+\beta)}\right]}{\left[1 - \frac{1+\beta}{\gamma(\alpha+\beta)}(h_{FE1}/h_{FE2})\right]} \frac{1}{I_{B1}}, \tag{50}$$

where α represents the ratio of the semiconductor resistance value, R_1, at low temperature, T_1, to that at a high temperature, T_2, $\beta = R_1/R_B$, $\gamma = V_{EB2}/V_{EB1}$, h_{FE1} and h_{FE2} represent the ratio of the transistor current

gains at low and high temperature and I_{B1} is the transistor base current at low temperature. The value of R_B so calculated will insure that the collector current at high temperature will just equal that set by I_{B1} at low temperature.

The derivation of Eq. (50) may be obtained by writing the following circuit equation, assuming $V_A = 1$ for simplicity:

$$V_A = 1 \tag{51a}$$

$$1 - V_{BE} = I_A R \tag{51b}$$

$$V_{BE} = I_B R \tag{51c}$$

$$I_A = I_B + I_R \tag{51d}$$

Combining these equations gives

$$I_R = \frac{1 - I_B R_B}{R + R_B} = \frac{(1/R_B - I_B)}{(1 + R/R_B)}.$$

If the device parameters and current values at the initial device temperature is denoted by the subscript 1 and the subscript 2 denotes a higher temperature that the device is suddenly raised to, we can write

$$\frac{I_{R1}}{I_{R2}} = \frac{(1/R_B - I_{B2})(1 + R_1/R_B)}{(1/R_B - I_{B1})(1 + R_2/R_B)}. \tag{52}$$

Defining $R_2 = R_1/\alpha$ and $R_B = R_1/\beta = \alpha R_2/\beta$, where α is determined by the temperature variation of the Ge resistor, Eq. (52) becomes

$$\frac{I_{R1}}{I_{R2}} = \left(\frac{1/R_B - I_{B2}}{1/R_B - I_{B1}}\right)\left(\frac{1 + \beta}{1 + \beta/\alpha}\right). \tag{53}$$

Now defining $\gamma = V_{BE2}/V_{BE1} = I_{R2}R_2/I_{R1}R_1 = I_{R2}/\alpha I_{R1}$, Eq. (53) can be written as

$$\frac{\gamma\alpha(1 + \beta/\alpha)}{(1 + \beta)} (1/R_B - I_{B1}) = (1/R_B - I_{B2}). \tag{54}$$

For stabilization let us require that $I_{C2} = I_{C1}$ so that $h_{FE1}I_{B1} = h_{FE2}I_{B2}$, using the definition of the grounded-emitter current gain, h_{FE}. The value of R_B required can now be written as in Eq. (50). R_1 is obtained from R_B after a value of β is chosen. From good current gain considerations β should be about 5 or more and α and γ are known from semiconductor theory, once the temperature dependence of h_{FE} is defined, so that all parameters are determined. As a sample calculation, let us assume that h_{FE} is temperature independent and $I_{C2} = I_{C1}$, then

$$\frac{I_{E1}}{I_{E2}} = 1 = \frac{De^{-(E_g - qV_{BE1})/\eta kT_1}}{De^{-(E_g - qV_{BE2})/\eta kT_2}}, \tag{55}$$

where D and η are assumed constant and independent of temperature. Solving for $\gamma = V_{BE2}/V_{BE1}$ yields

$$\frac{V_{BE2}}{V_{BE1}} = \frac{T_2}{T_1} - \left(\frac{T_2}{T_1} - 1\right)E_g/qV_{BE1}, \tag{56}$$

and assuming $E_g \approx 2qV_{BE1}$ for silicon junctions,

$$\gamma = V_{BE2}/V_{BE1} \approx (2 - T_2/T_1),$$

so that γ can be calculated.

The details of the practical implementation of this invention are being pursued.

V. REFERENCES

[1] H.A. Schafft, "Second Breakdown-A Comprehensive Review," Proc. IEEE Vol. 55, pp. 1272-1288, August 1967.

[2] D. Navon and E.A. Miller, "Thermal Stability in Power Transistor Structures," Solid State Elect. Vol. 12, pp. 69-78, Feb. 1969.

[3] D. Navon and R.E. Lee, "Effect of Non-Uniform Emitter Current Distribution on Power Transistor Stability," Solid-State Elect. Vol. 13, pp. 981-991 July 1970.

[4] T.R. Schlax, "A Study of the Potential, Current, and Charge Distribution within the Transistor Base Region," Ph.D. Dissertation, Department of Electrical Engineering, MIT October 1967.

[5] D.L. Smythe, "Hole and Electron Mobility in Semiconductor with Large Number of Excess Carriers," Ph.D. Dissertation, Department of Electrical Engineering, MIT, February 1967.

[6] R.D. Thornton, P. DeWitt, E.R. Chenette and P.E. Gray, "Characteristics and Limitations of Transistors," John Wiley and Sons, Inc. New York 1966.

[7] F.B. Hilderbrand, "Finite Difference Equations and Simulations," Prentice Hall, Inc., Englewood Cliffs, N.J. 1968.

[8] C.J. Glassbrenner and G.A. Slack, "Thermal Conductivity of Silicon and Germanium from 3°K to the Melting Point," Phys. Rev., Vol. 134 pp. A1058-A1069, May 1964.

[9] S.P. Gaur, D. Navon and R.W. Teerlinck, "Transistor Design and Thermal Stability," to be submitted for publication in IEEE Trans. on Electron Devices.

[10] R.B. Adler, A.C. Smith and R.L. Longini, "Introduction to Semiconductor Physics," John Wiley and Sons. Inc. New York 1964.

[11] J.C. Irvin, "Resistivity of Bulk Silicon and of Diffused Layers in Silicon," Bell Sys. Tech. J., Vol. 41, pp. 387-410, March 1962.

[12] M. Lauriente and J.L. Fergason, "Liquid Crystals Plot the Hot Spots," Electron.Design, Vol. 19, pp. 71-79, Sept. 13, 1967.

VI. Conclusions and Future Work

A technique has been developed for the theoretical analysis of the thermal behavior of various power transistor structures operating in the active region at low frequencies. Computation of the electric current and heat flow problem yields a prediction of the steady-state temperature and current distribution in a given interdigited transistor design. Should the specified operating power be to high, excessively elevated temperatures will be predicted and the semiconductor material will be raised into its "intrinsic" range, resulting in ordinary thermal runaway. In addition, a device operating normally in the steady-state, at a relatively high power level, can become unstable if a spurious temperature rise occurs somewhere in the transistor chip. For then a "lateral" thermal instability may be predicted causing a very local concentration of current at the hot spot and resulting in a continuously increasing temperature there, in time. This constitutes a model for forward second breakdown. A study of the effect of device design parameters such as chip thickness, base width, emitter width, base impurity concentration, etc., on thermal stability has yielded information which may be used to optimize power transistor design.

Experimental probing of the transistor temperature distribution, using cholesteric liquid crystals, coupled with voltage probing along emitter fingers has yielded information on the temperature and current distributions in a DC operating device. Actual DC and pulse testing of transistors has supplied data on the maximum power capability of commercial devices, particularly versus case temperature.

Future work will include the following areas:

1. Theoretical evaluation of the temperature sensing germanium resistor method of transistor thermal stabilization versus the ordinary emitter resistor ballasting scheme.

2. A coupling of the technique of liquid crystal temperature probing with the second breakdown test circuit, in order to pursue thermal studies near the device instability point.

3. An extension of the theoretical study of thermal instability to high frequency and pulsed transistor operation.